FIG. 1
PRIOR ART

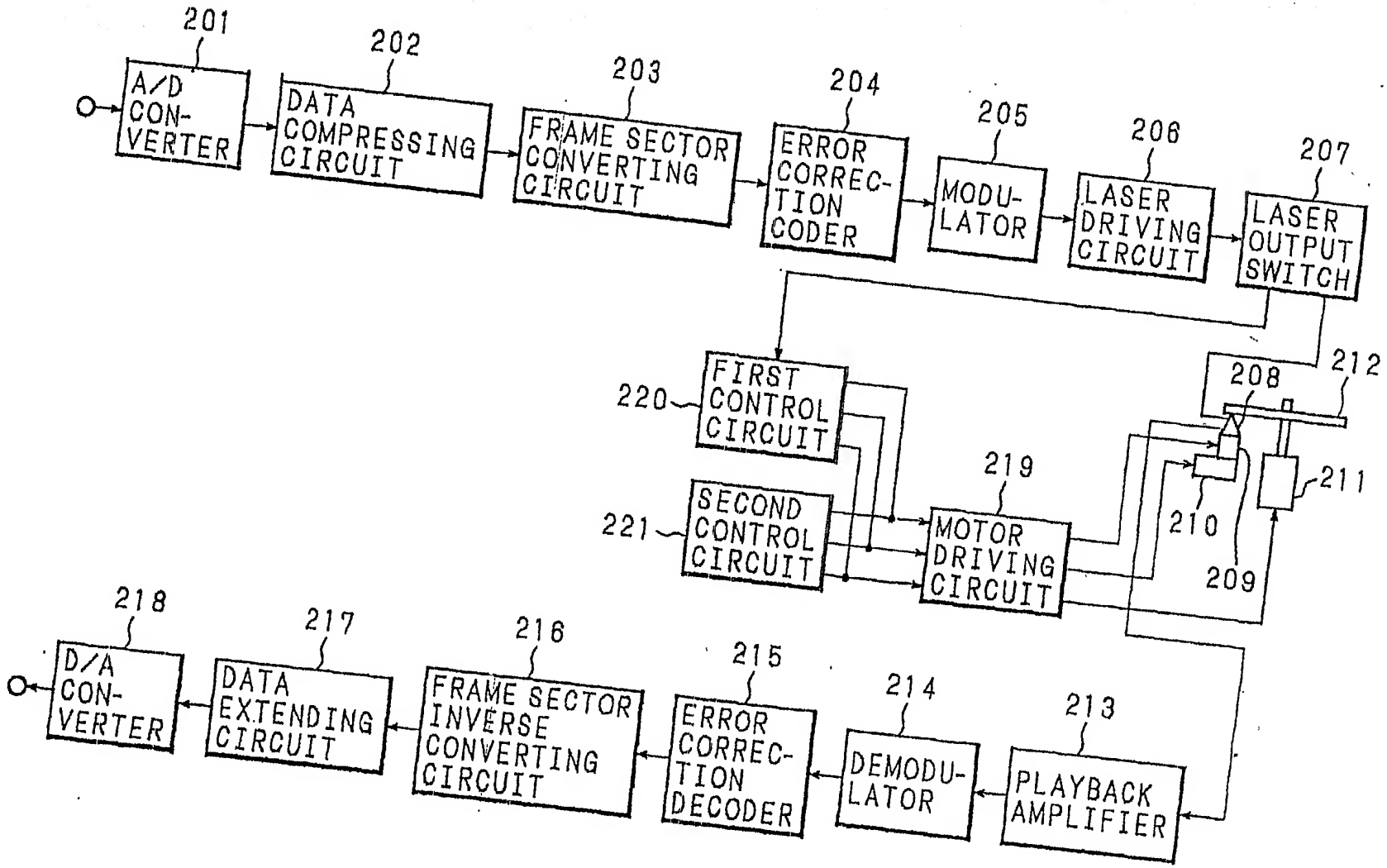


FIG. 2
PRIOR ART

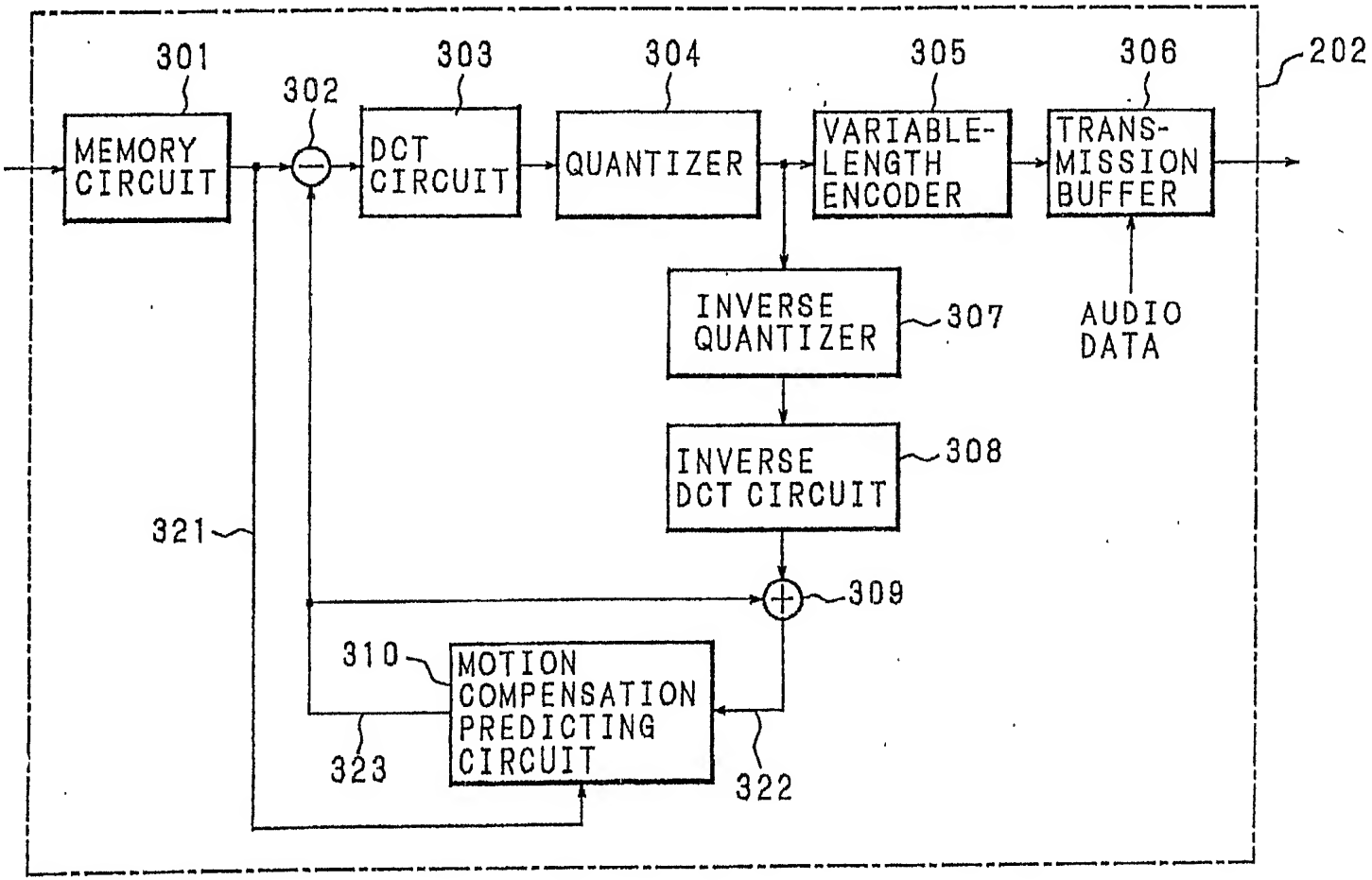


FIG. 3
PRIOR ART

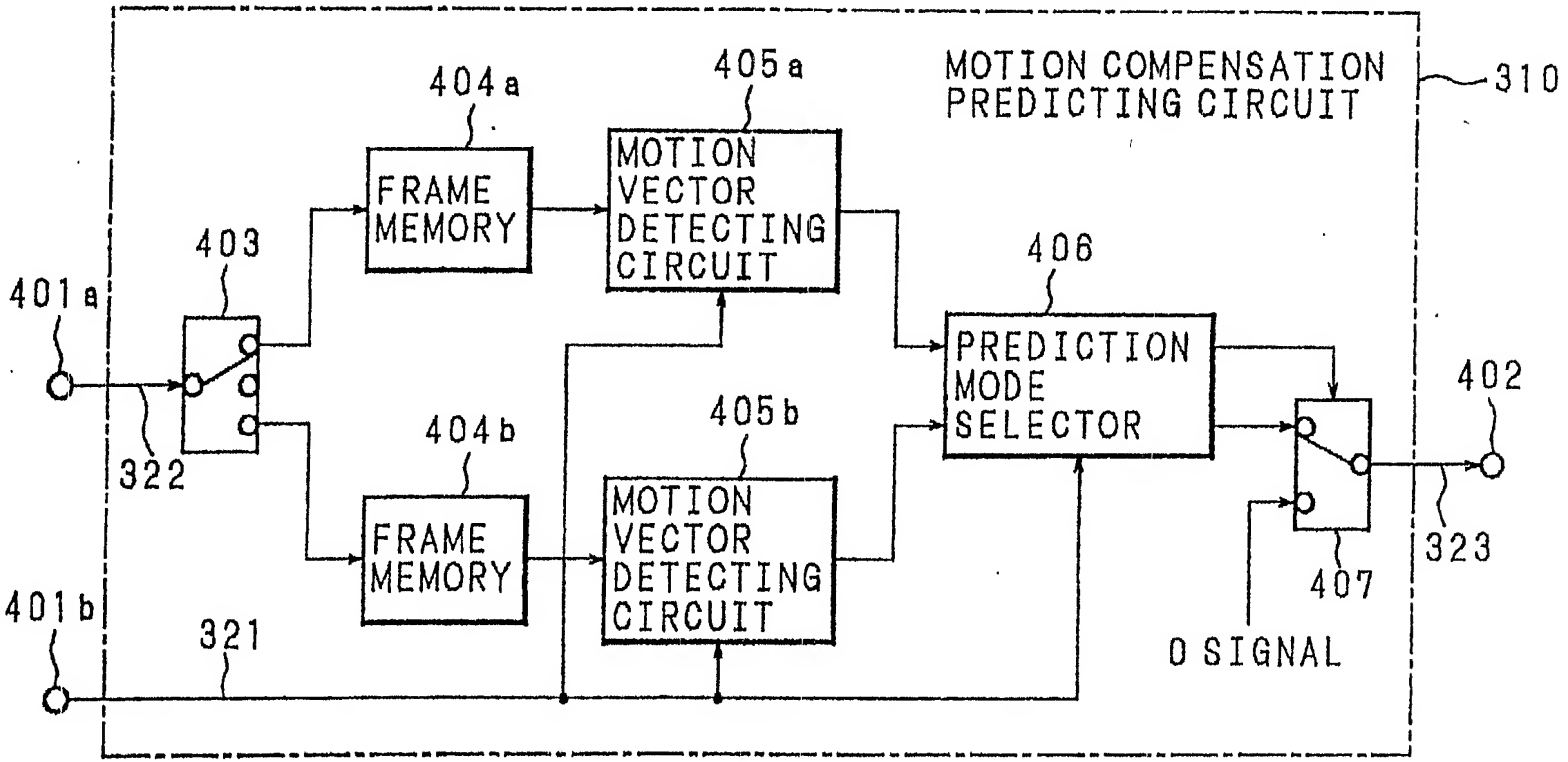


FIG. 4
PRIOR ART

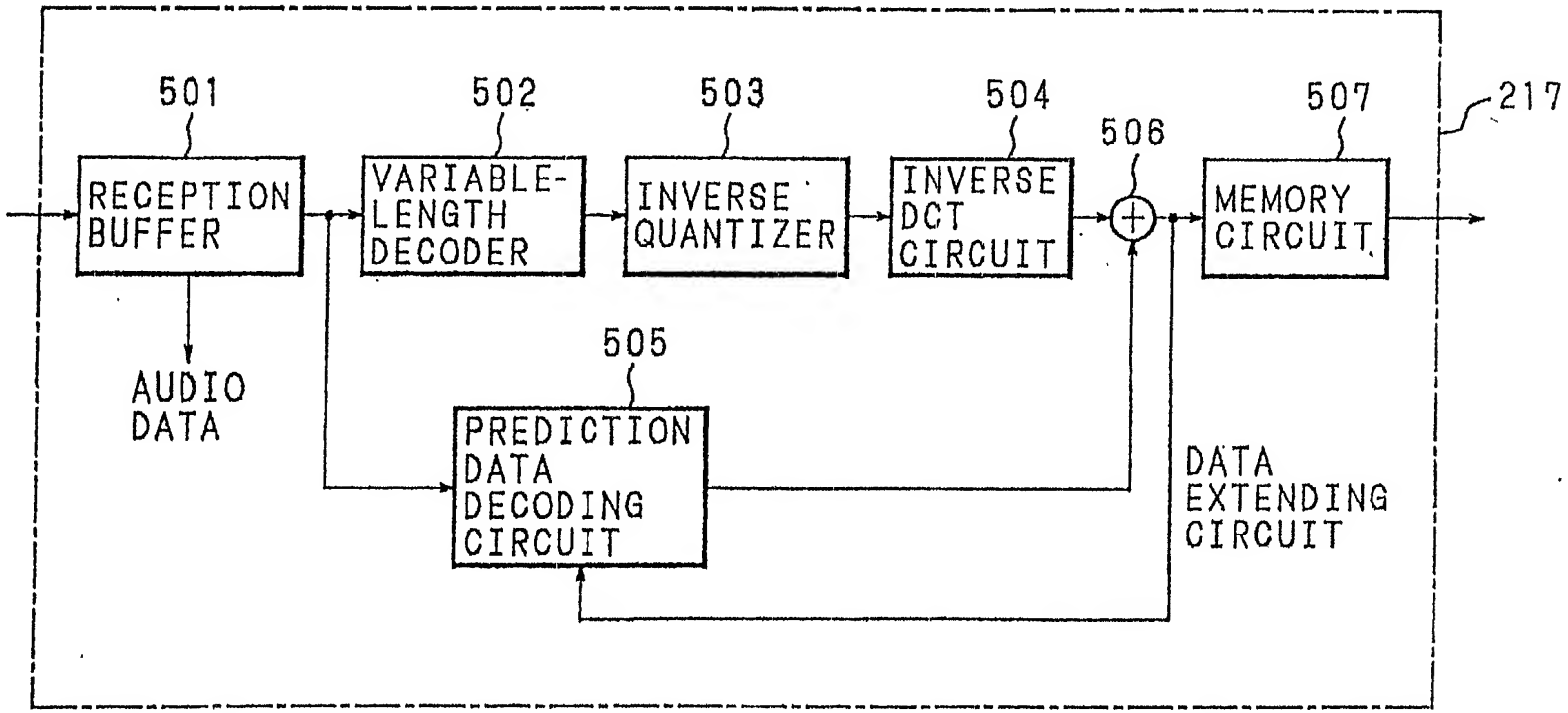


FIG. 5
PRIOR ART

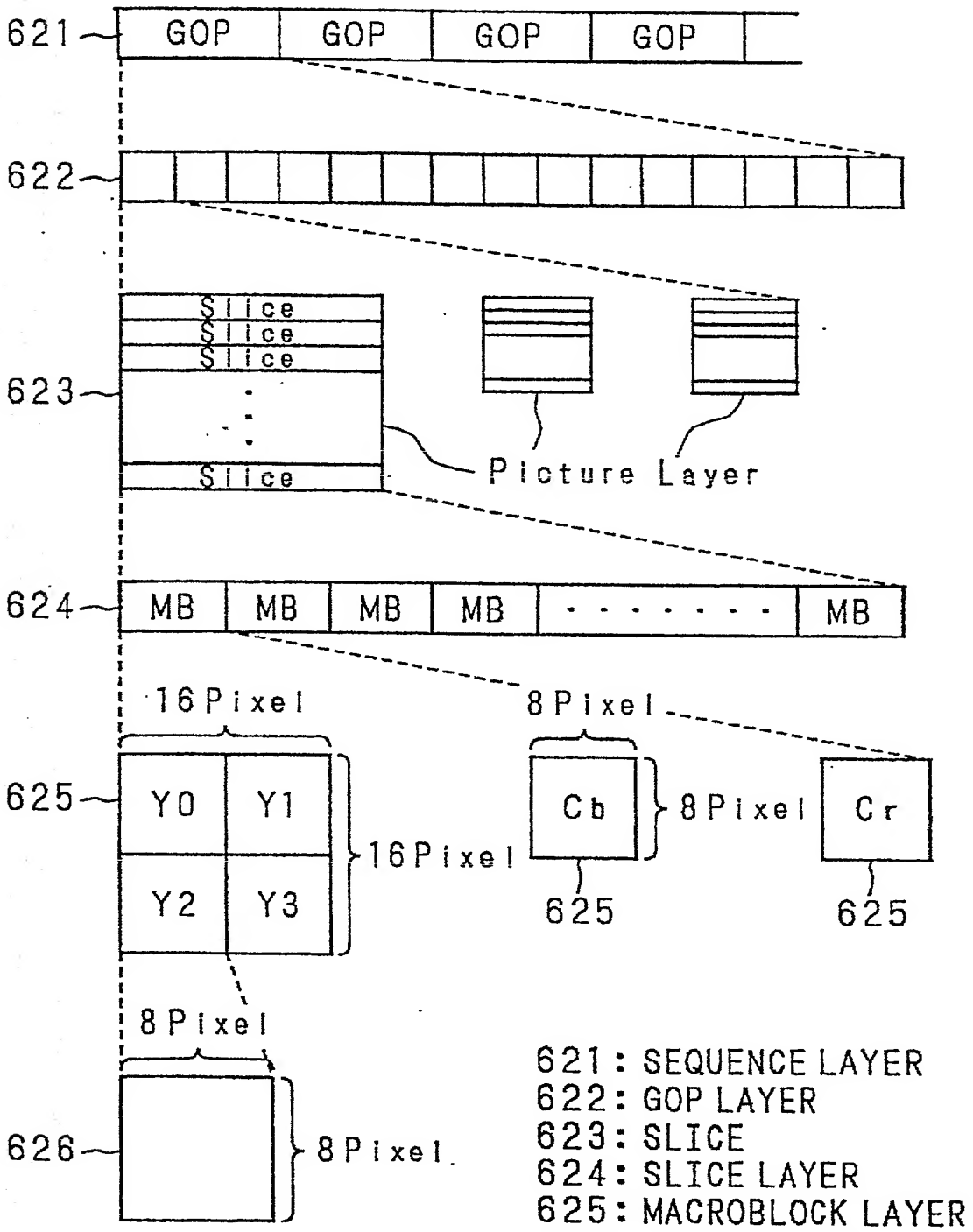


FIG. 6
PRIOR ART

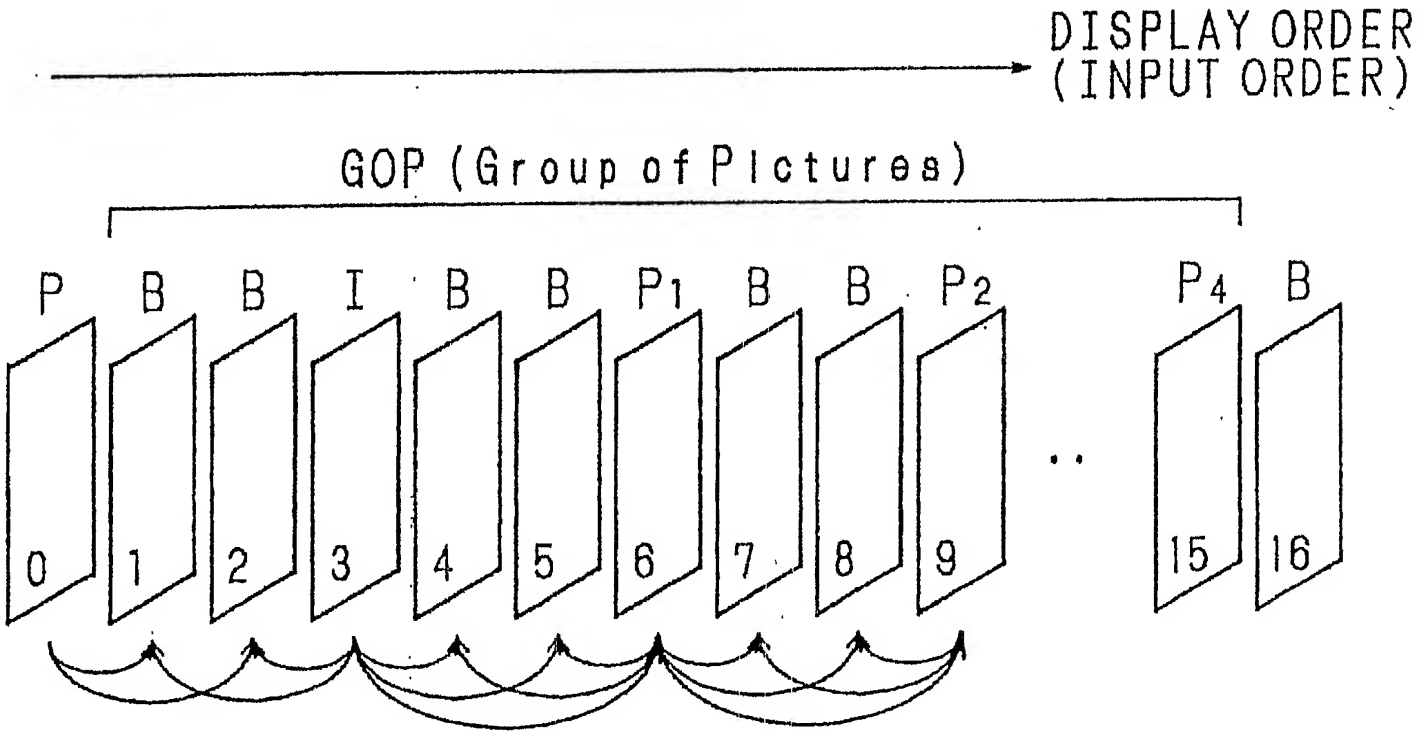


FIG. 7A
PRIOR ART

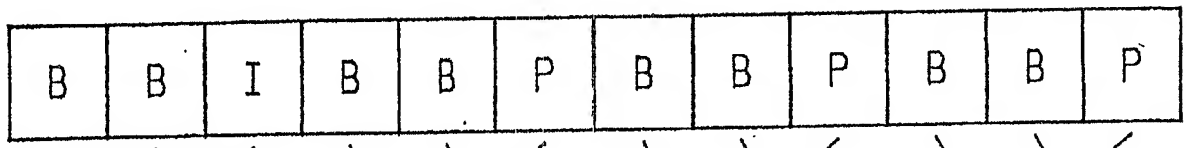


FIG. 7B
PRIOR ART

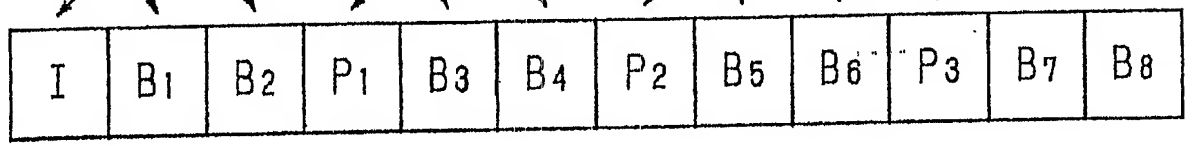


FIG. 8
PRIOR ART

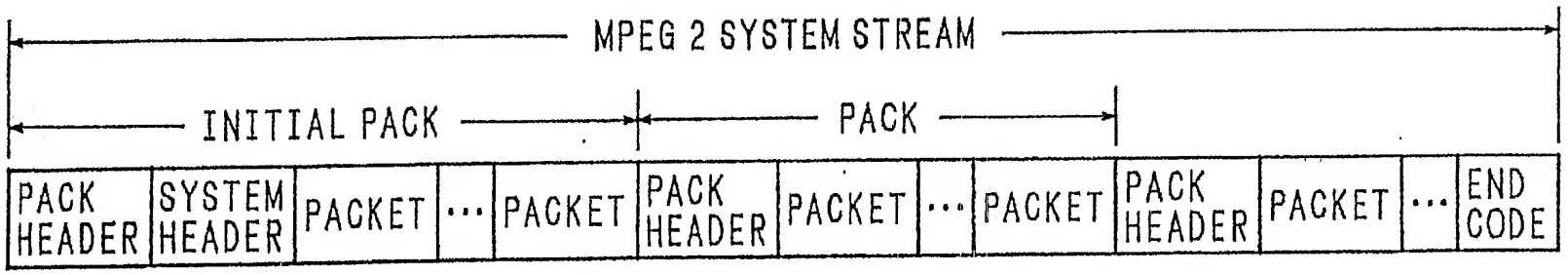


FIG. 9
PRIOR ART

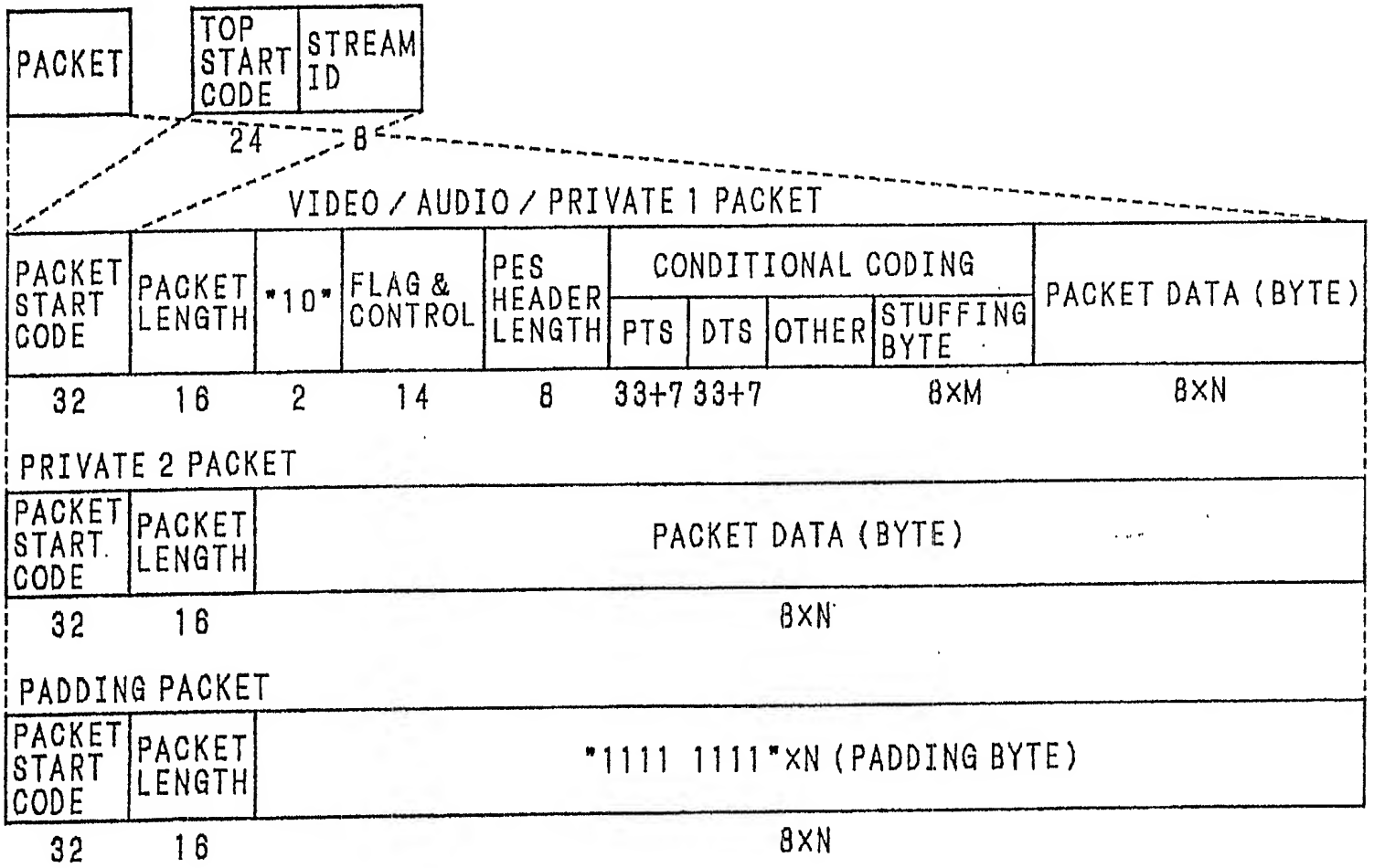


FIG. 10
PRIOR ART

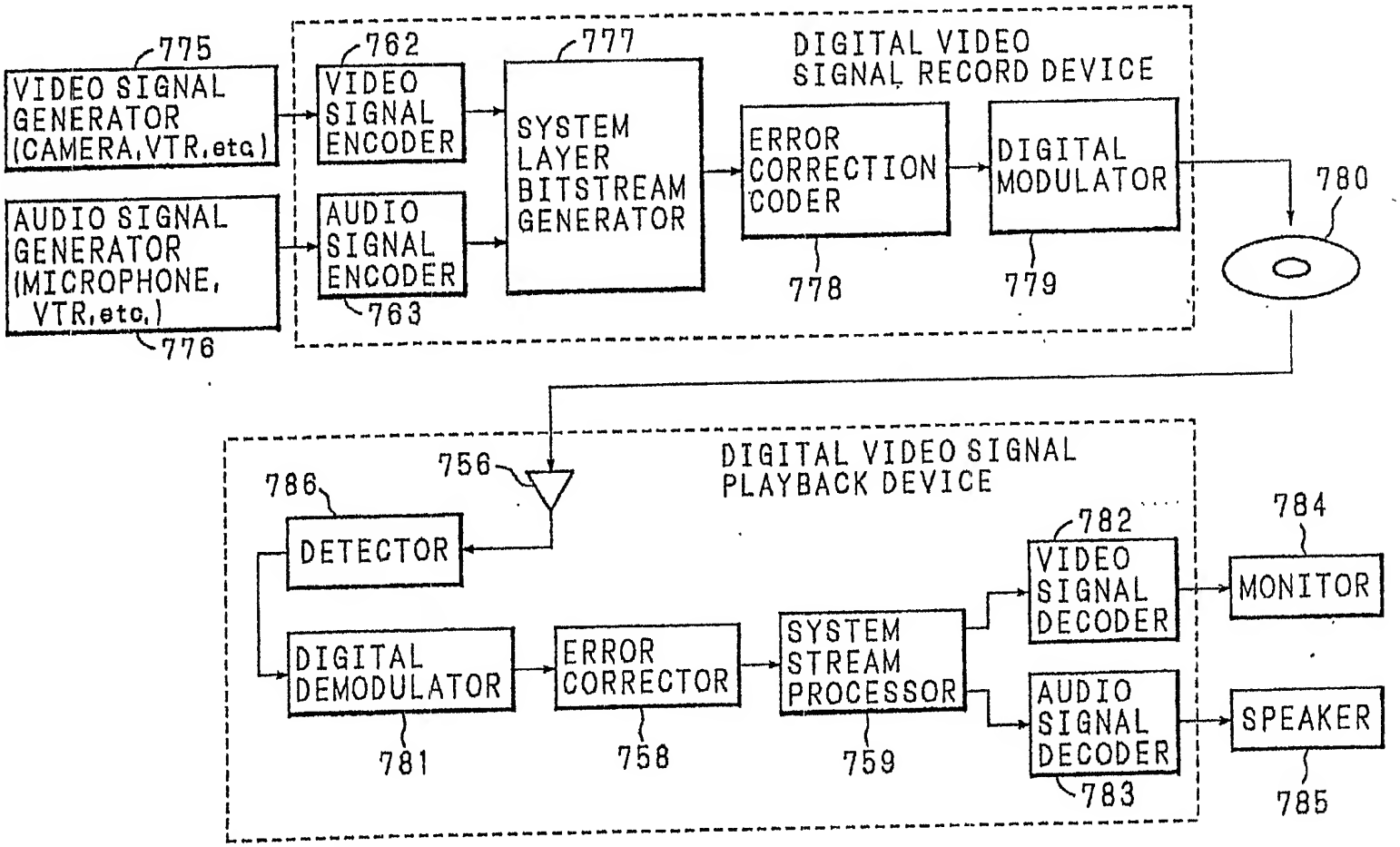


FIG. 11
PRIOR ART

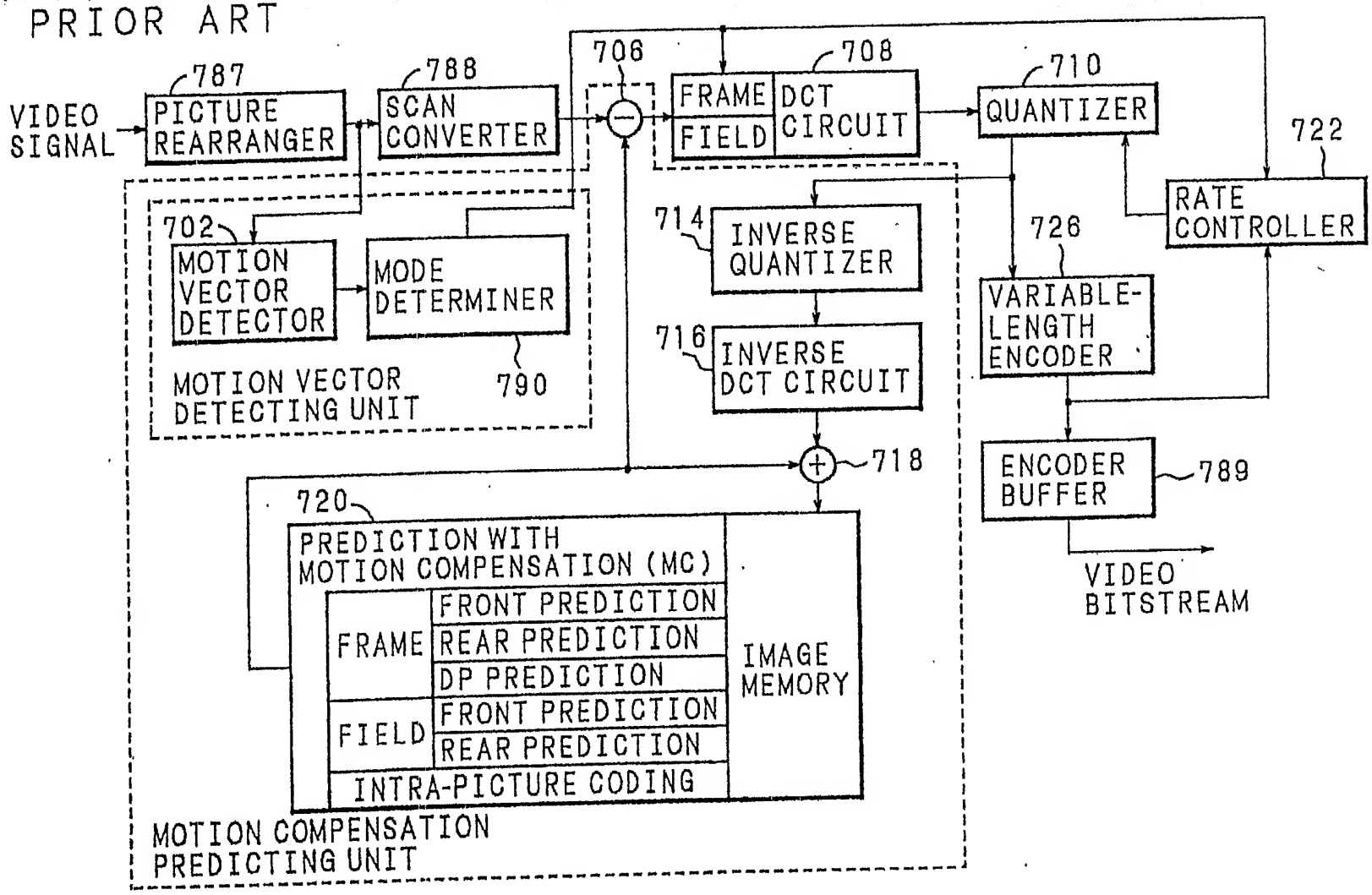


FIG. 12
PRIOR ART

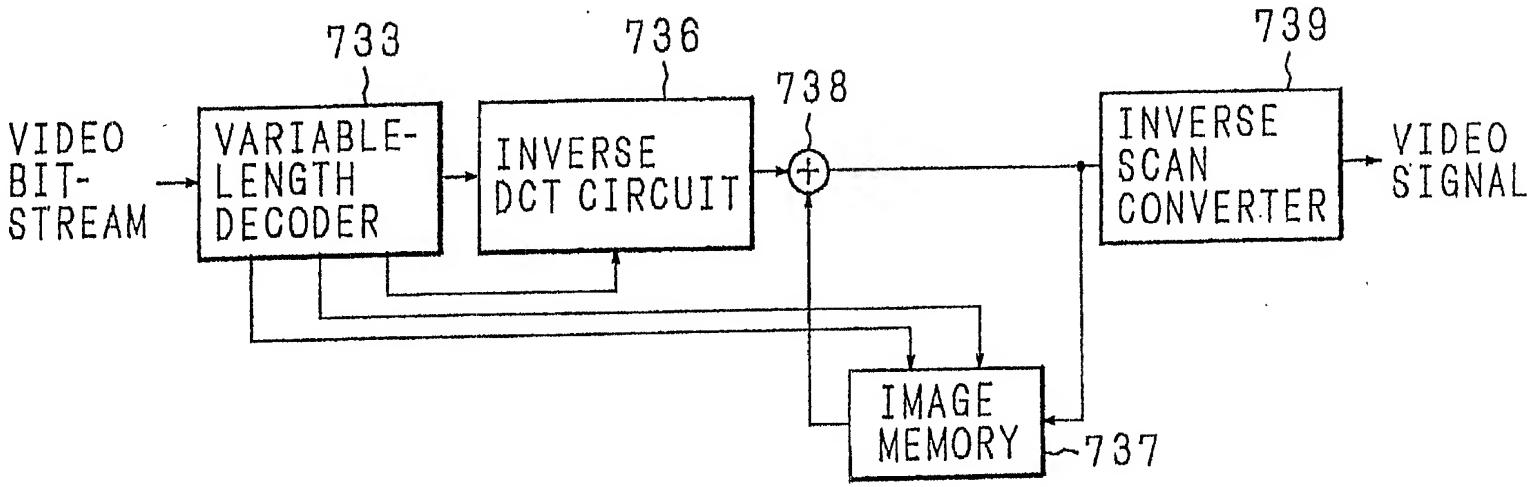
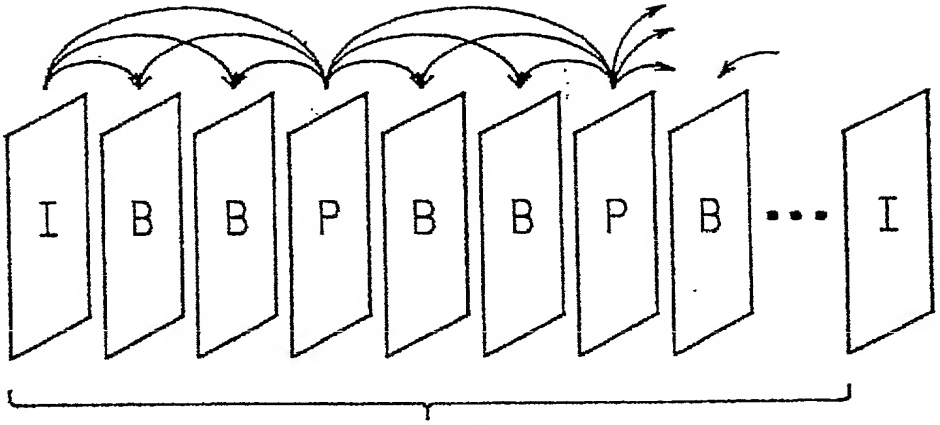


FIG. 13A
PRIOR ART



I:I-PICTURE
P:P-PICTURE
B:B-PICTURE

ARROW SHOWING PREDICTION

FIG. 13B
PRIOR ART

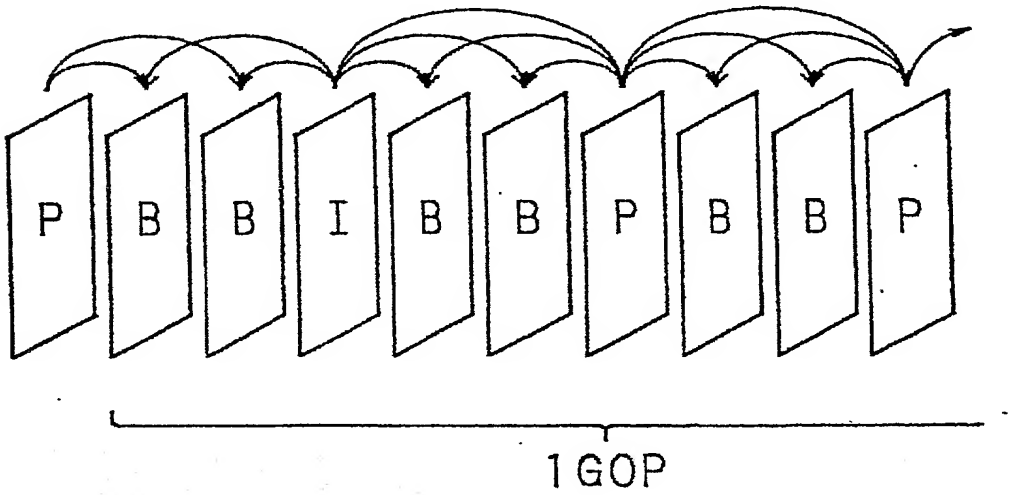


FIG. 14
PRIOR ART

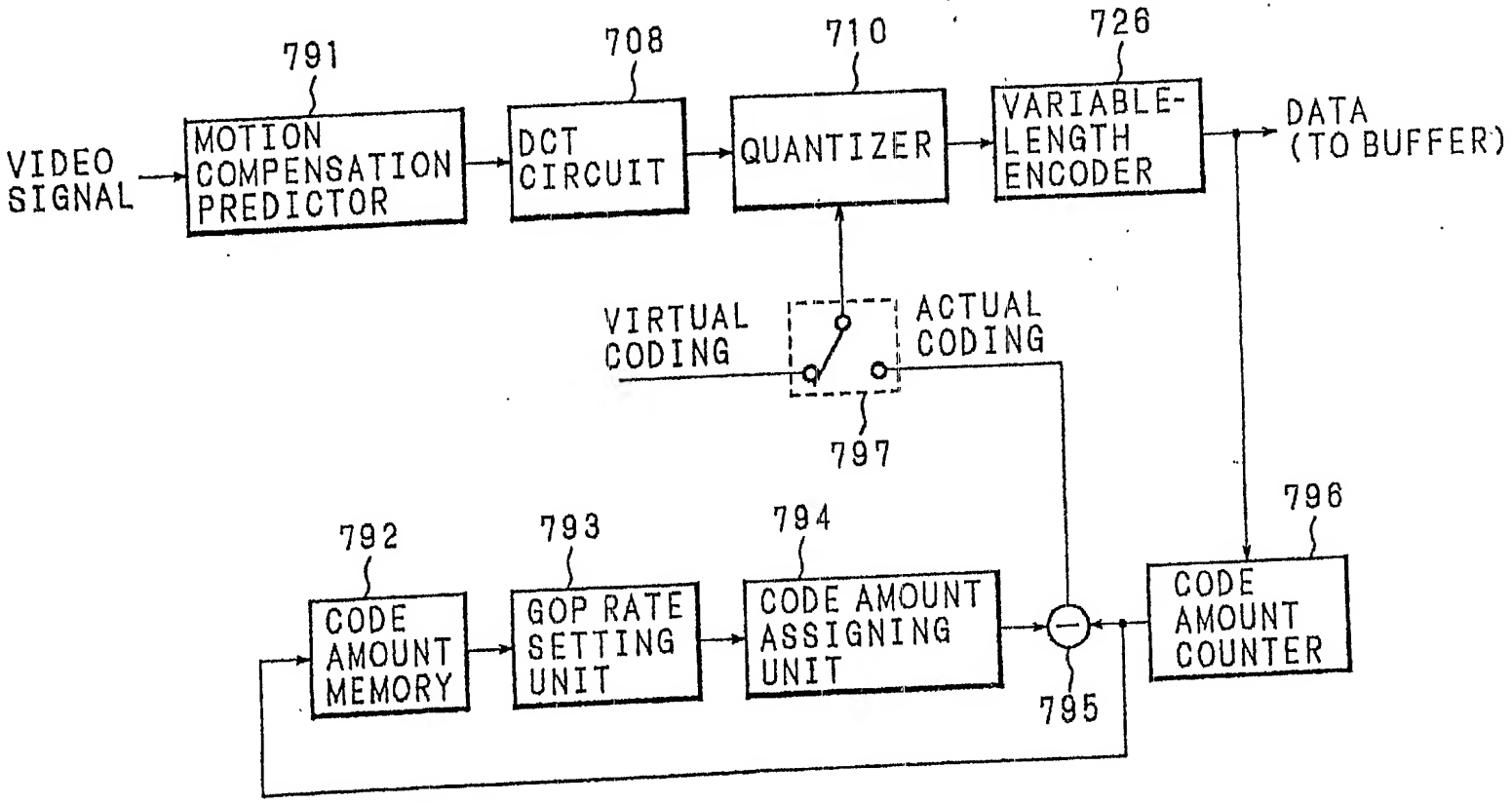


FIG. 15

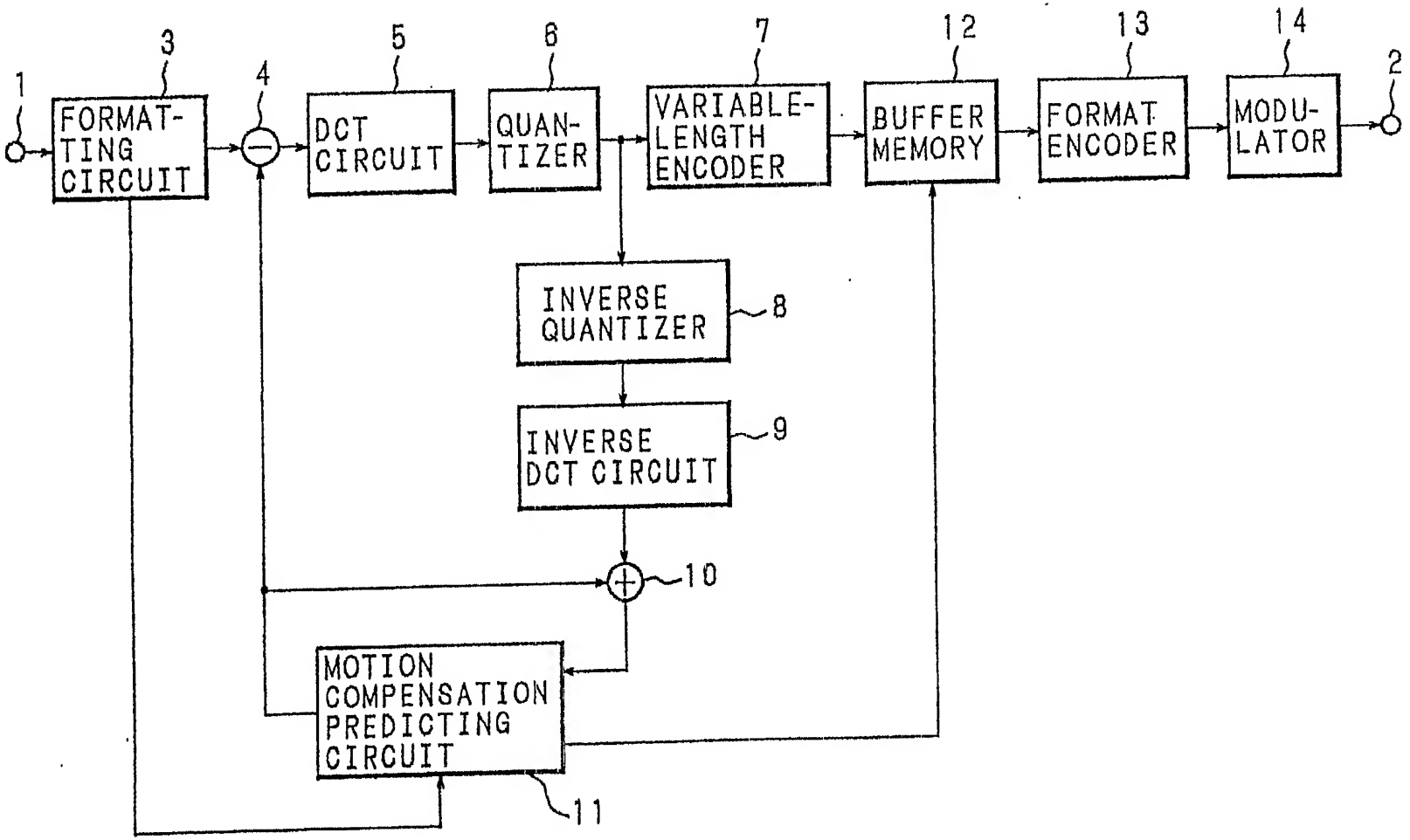

1
3
FORMAT-TING CIRCUIT
4
5
DCT CIRCUIT
6
QUAN-TIZER
7
VARIABLE-LENGTH ENCODER
12
BUFFER MEMORY
13
FORMAT ENCODER
14
MODU-LATOR
2
INVERSE QUANTIZER
8
INVERSE DCT CIRCUIT
9
10
MOTION COMPENSATION PREDICTING CIRCUIT
11

FIG. 16

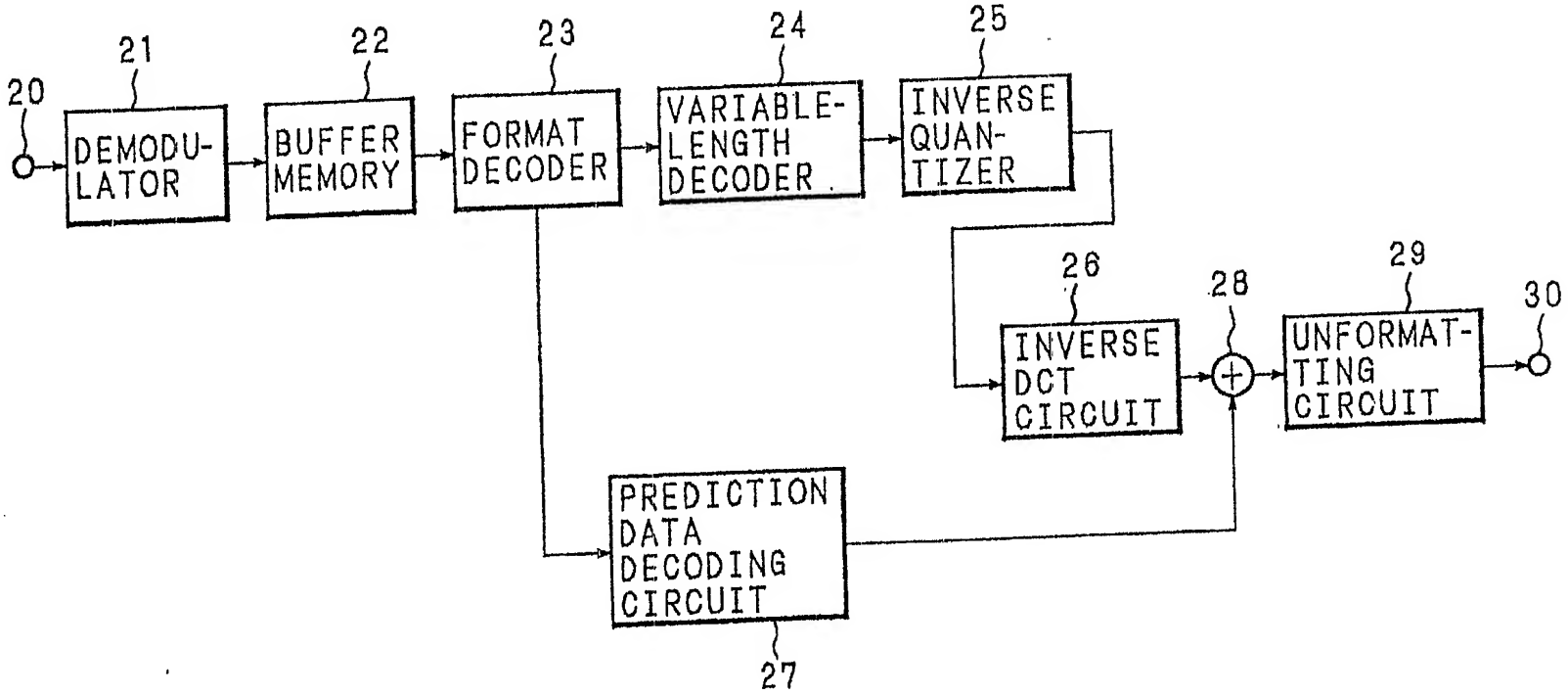

20
21
DEMODU-
LATOR
22
BUFFER
MEMORY
23
FORMAT
DECODER
24
VARIABLE-
LENGTH
DECODER
25
INVERSE
QUAN-
TIZER
26
INVERSE
DCT
CIRCUIT
28
29
UNFORMAT-
TING
CIRCUIT
30
PREDICTION
DATA
DECODING
CIRCUIT
27

FIG. 17.

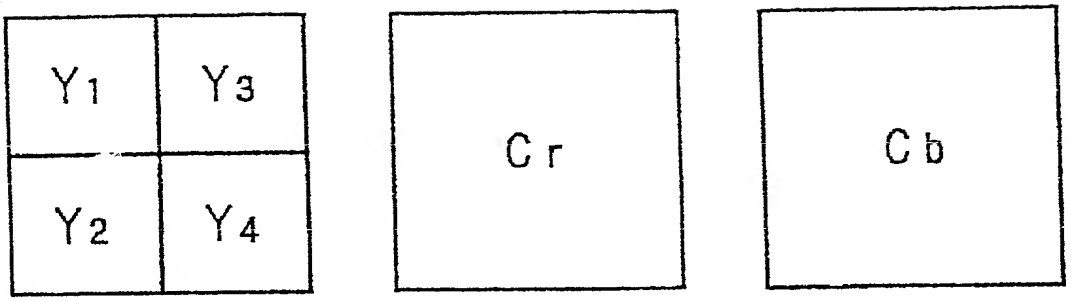


FIG. 18

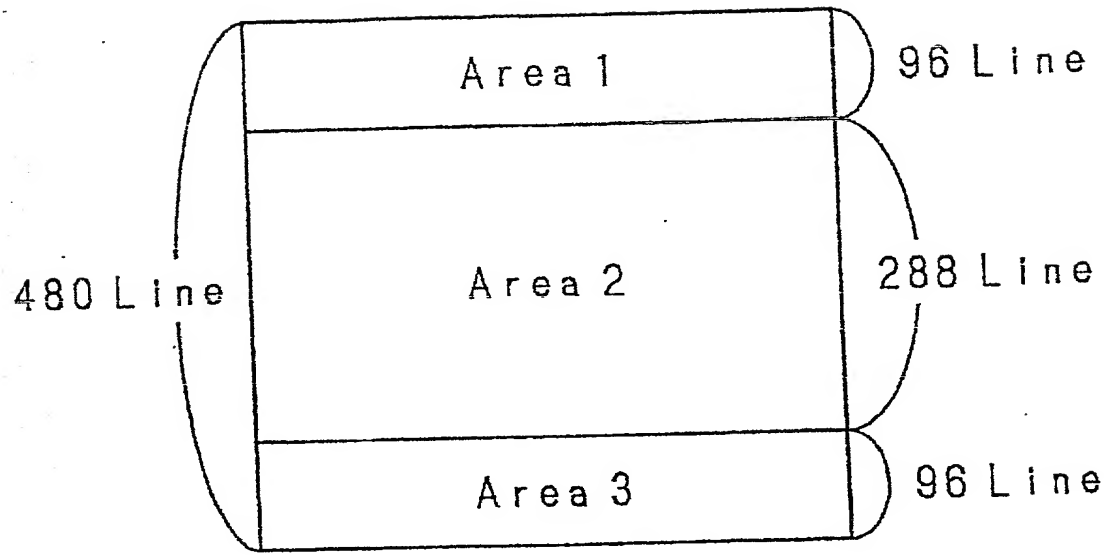


FIG. 19

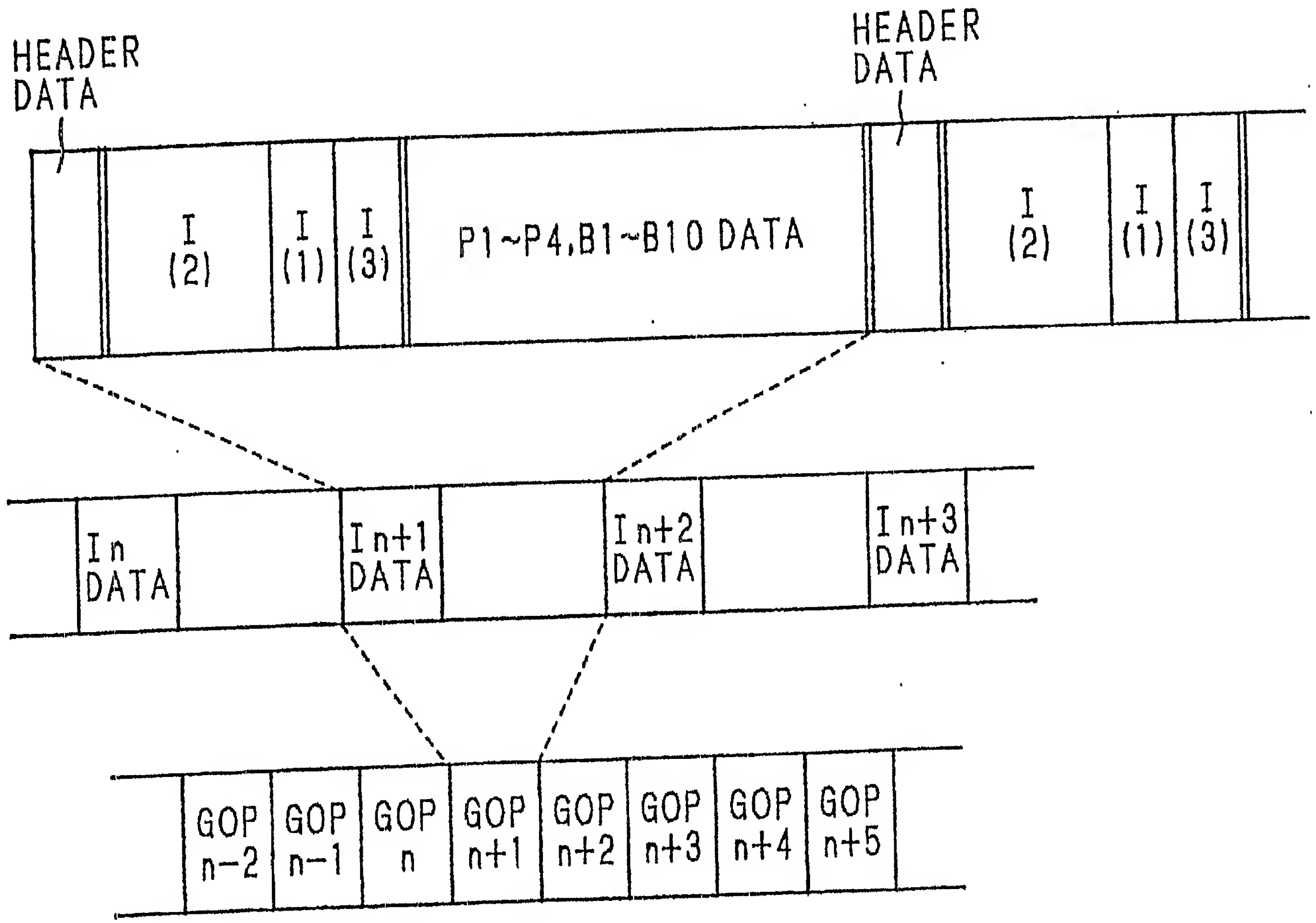
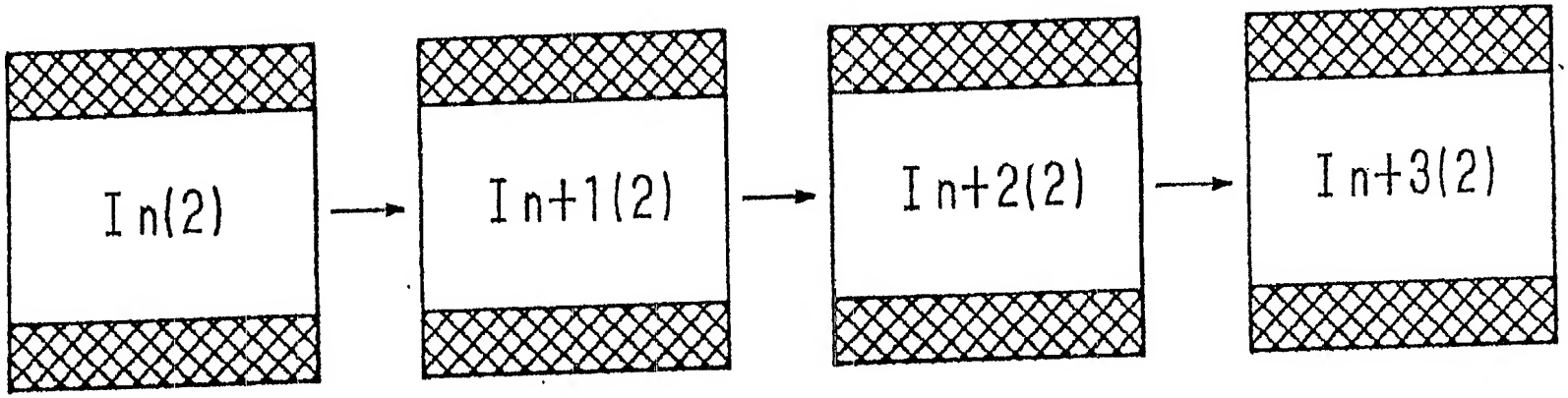

HEADER DATA
I (2)
I (1)
I (3)
P1~P4,B1~B10 DATA
HEADER DATA
I (2)
I (1)
I (3)
In DATA
In+1 DATA
In+2 DATA
In+3 DATA
GOP n−2
GOP n−1
GOP n
GOP n+1
GOP n+2
GOP n+3
GOP n+4
GOP n+5

FIG. 20A FIG. 20B FIG. 20C FIG. 20D




:MASK DATA

FIG. 21A

FIG. 21B

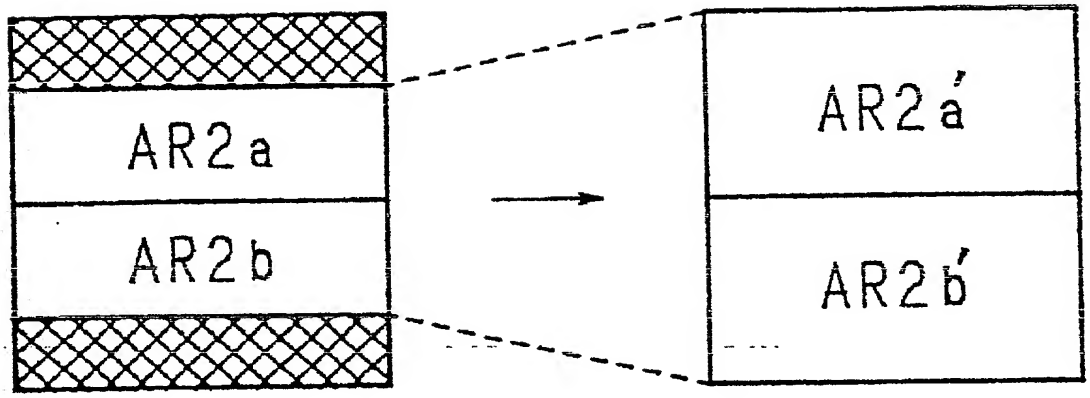


FIG. 22

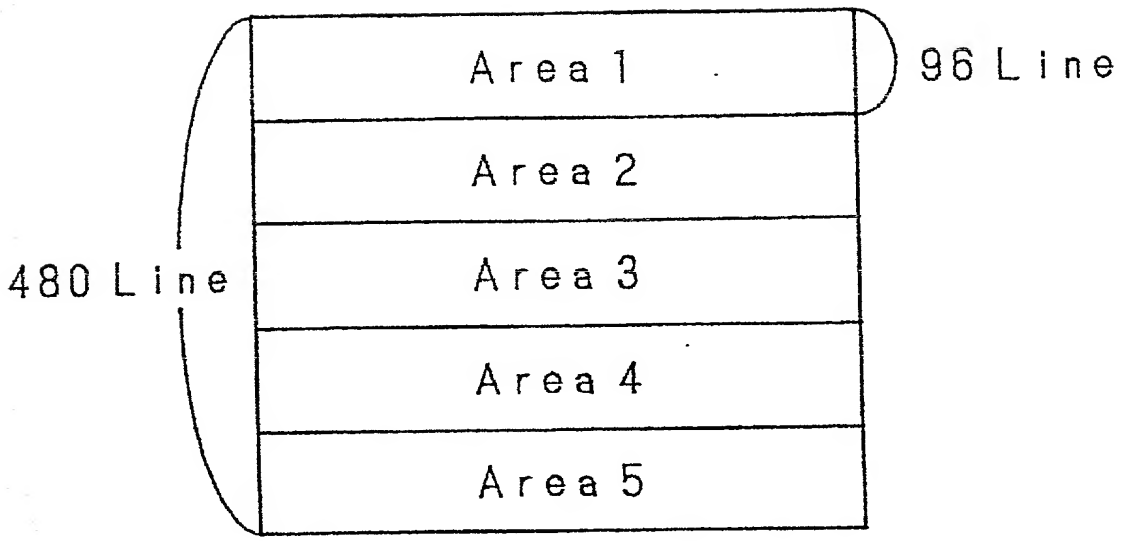


FIG. 23

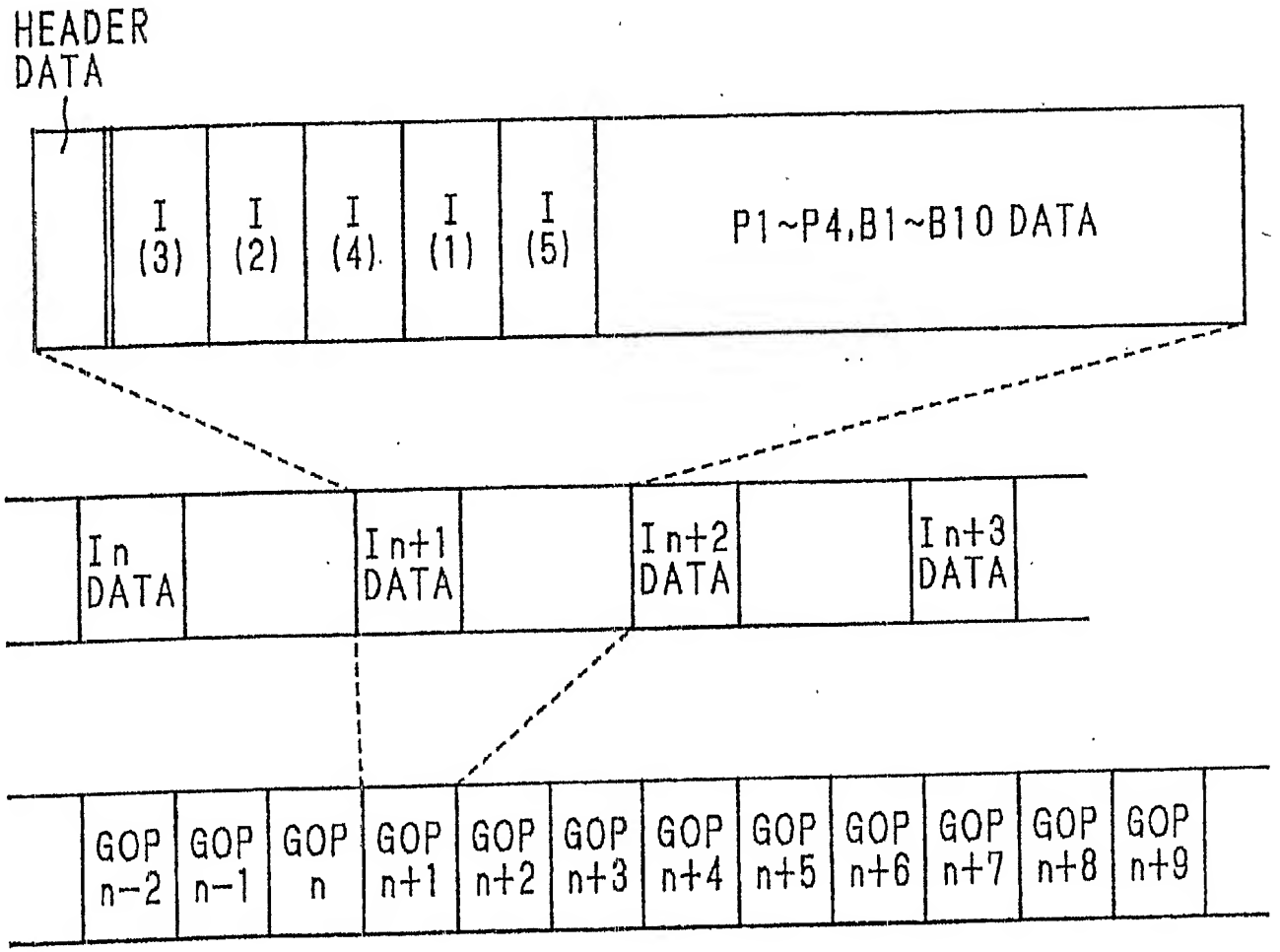

HEADER DATA
I (3)
I (2)
I (4)
I (1)
I (5)
P1~P4,B1~B10 DATA
In DATA
In+1 DATA
In+2 DATA
In+3 DATA
GOP n-2
GOP n-1
GOP n
GOP n+1
GOP n+2
GOP n+3
GOP n+4
GOP n+5
GOP n+6
GOP n+7
GOP n+8
GOP n+9

FIG. 24A FIG. 24B FIG. 24C FIG. 24D FIG. 24E

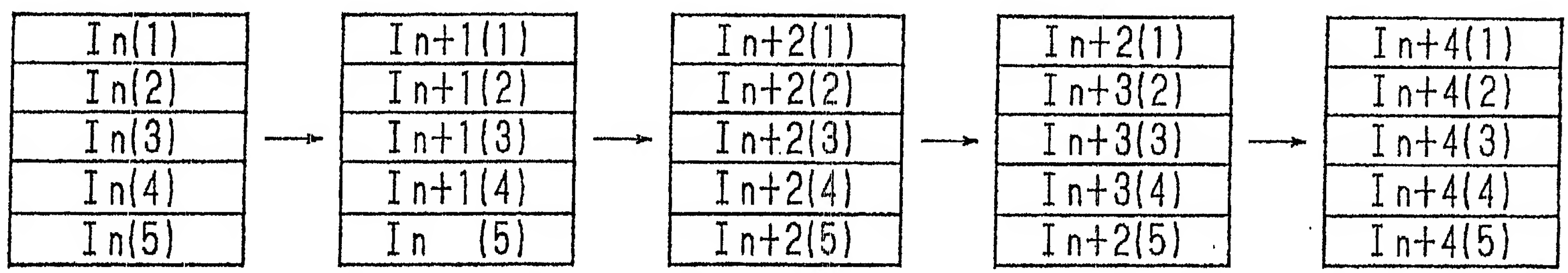


FIG. 25A

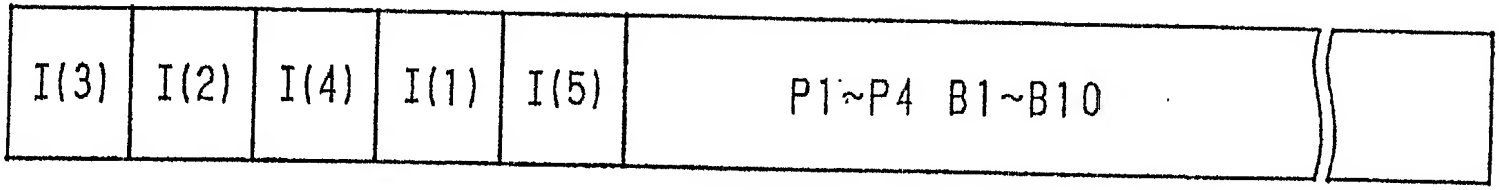


FIG. 25B

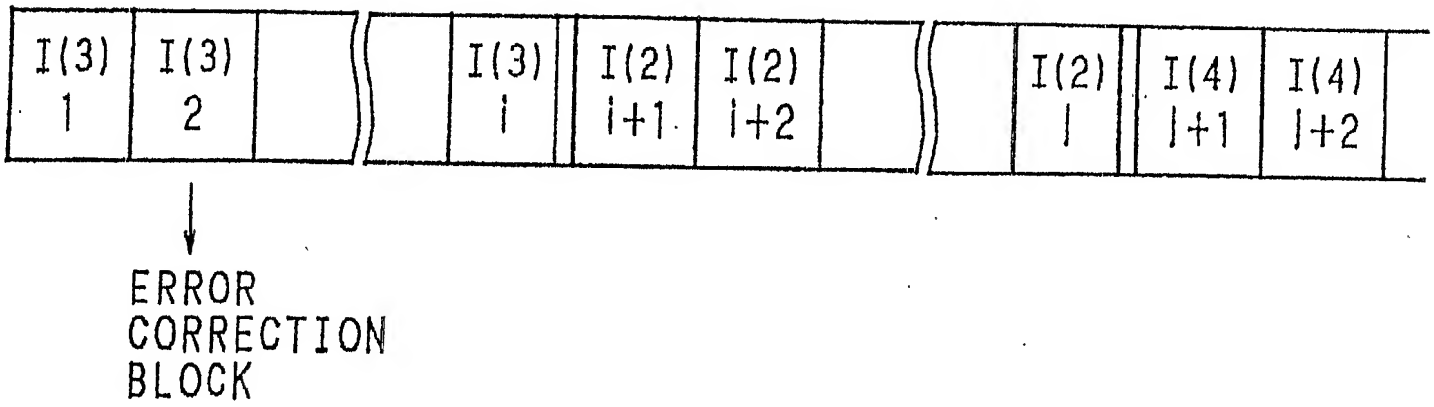


FIG. 26A

In+4(1)
In+3(2)
In+2(3)
In+1(4)
In (5)

FIG. 26B

In+5(1)
In+4(2)
In+3(3)
In+2(4)
In+1(5)

FIG. 26C

In+6(1)
In+5(2)
In+4(3)
In+3(4)
In+2(5)

FIG. 26D

In+7(1)
In+6(2)
In+5(3)
In+4(4)
In+3(5)

FIG. 27A

In+2(1)
In+1(2)
In (3)
In−1(4)
In−2(5)

FIG. 27B

In+2(1)
In+2(2)
In+1(3)
In (4)
In−1(5)

FIG. 27C

In+4(1)
In+3(2)
In+2(3)
In+1(4)
In (5)

FIG. 27D

In+5(1)
In+4(2)
In+3(3)
In+2(4)
In (5)

FIG. 27E

In+6(1)
In+5(2)
In+4(3)
In+3(4)
In+2(5)

FIG. 27F

In+7(1)
In+6(2)
In+5(3)
In+4(4)
In+3(5)

FIG. 28

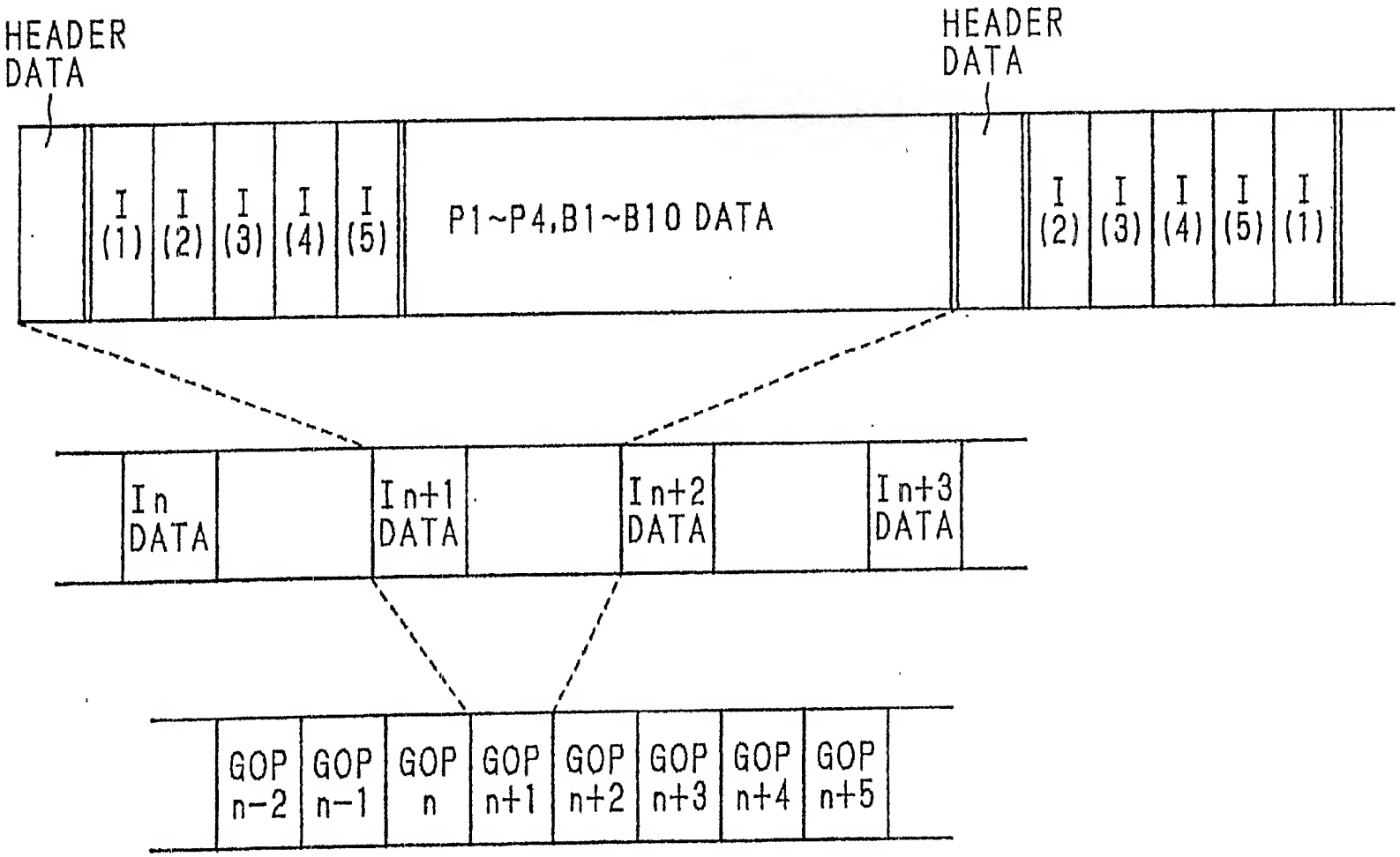

HEADER DATA
HEADER DATA
I (1)
I (2)
I (3)
I (4)
I (5)
P1~P4,B1~B10 DATA
I (2)
I (3)
I (4)
I (5)
I (1)
In DATA
In+1 DATA
In+2 DATA
In+3 DATA
GOP n-2
GOP n-1
GOP n
GOP n+1
GOP n+2
GOP n+3
GOP n+4
GOP n+5

FIG. 29A

In(1)
In(2)
In(3)
In(4)
In(5)

FIG. 29B

In+1(1)
In+1(2)
In+1(3)
In+1(4)
In (5)

FIG. 29C

In+2(1)
In+2(2)
In+2(3)
In+2(4)
In+2(5)

FIG. 29D

In+2(1)
In+2(2)
In+3(3)
In+3(4)
In+3(5)

FIG. 29E

In+4(1)
In+4(2)
In+4(3)
In+4(4)
In+4(5)

FIG. 30

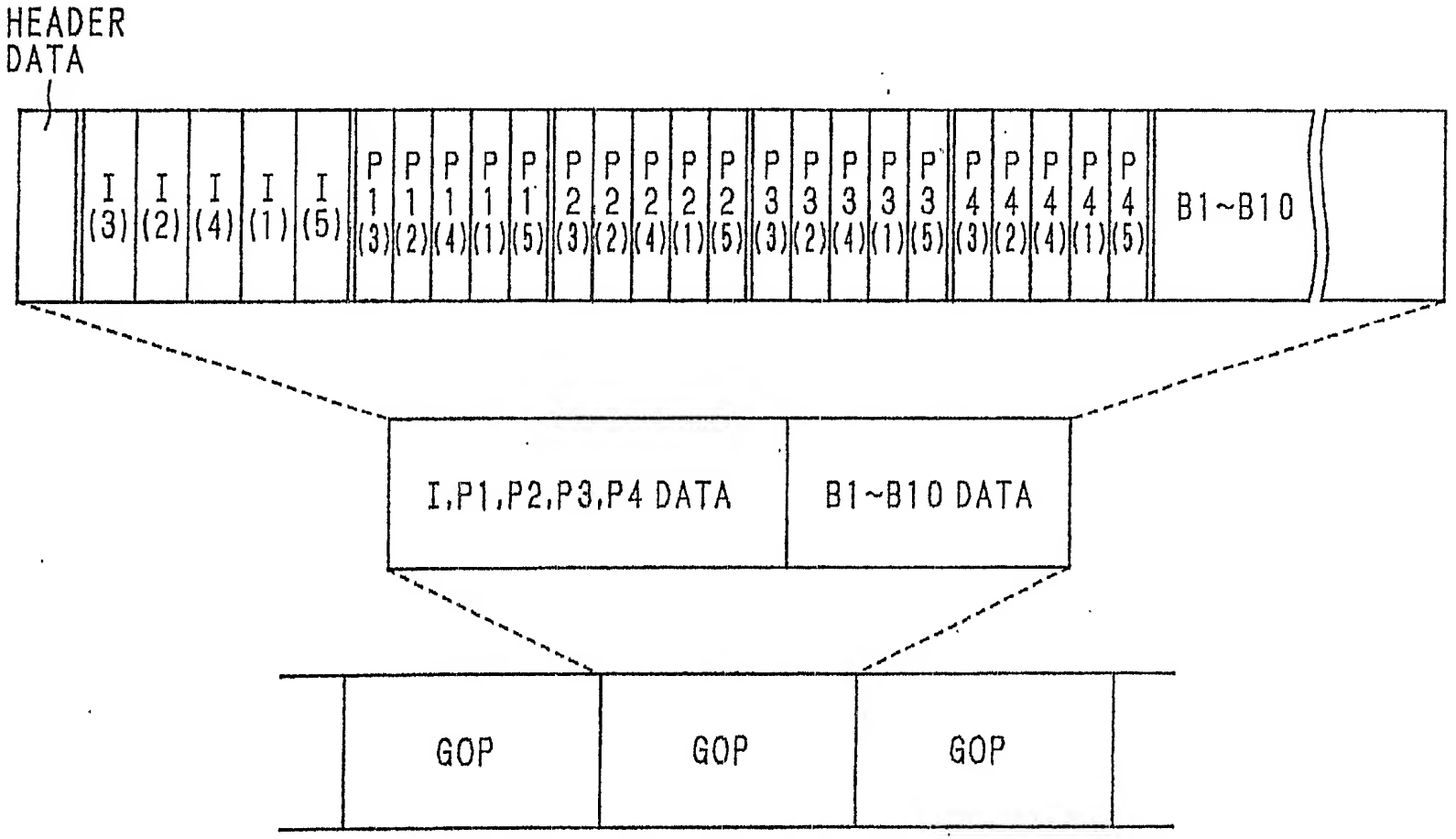

HEADER DATA
I (3)
I (2)
I (4)
I (1)
I (5)
P 1 (3)
P 1 (2)
P 1 (4)
P 1 (1)
P 1 (5)
P 2 (3)
P 2 (2)
P 2 (4)
P 2 (1)
P 2 (5)
P 3 (3)
P 3 (2)
P 3 (4)
P 3 (1)
P 3 (5)
P 4 (3)
P 4 (2)
P 4 (4)
P 4 (1)
P 4 (5)
B1~B10
I,P1,P2,P3,P4 DATA
B1~B10 DATA
GOP
GOP
GOP

FIG. 31A

In(1)
In(2)
In(3)
In(4)
In(5)

FIG. 31B

P1n(1)
P1n(2)
P1n(3)
P1n(4)
P1n(5)

FIG. 31C

P2n(1)
P2n(2)
P2n(3)
P2n(4)
P2n(5)

FIG. 31D

P3n(1)
P3n(2)
P3n(3)
P3n(4)
P3n(5)

FIG. 31E

P3n(1)
P4n(2)
P4n(3)
P3n(4)
P3n(5)

FIG. 31F

In+1(1)
In+1(2)
In+1(3)
In+1(4)
In+1(5)

FIG. 32A

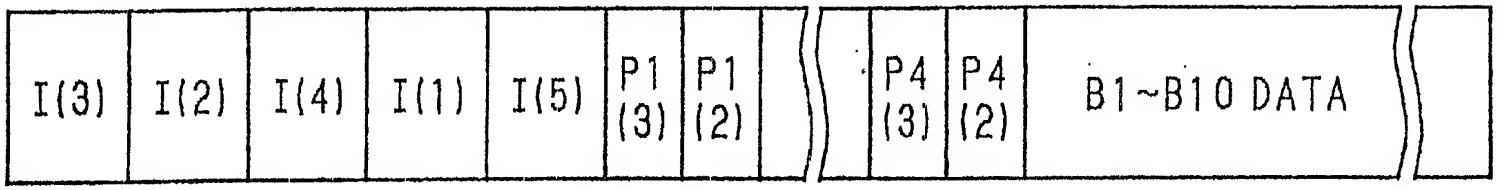


FIG. 32B

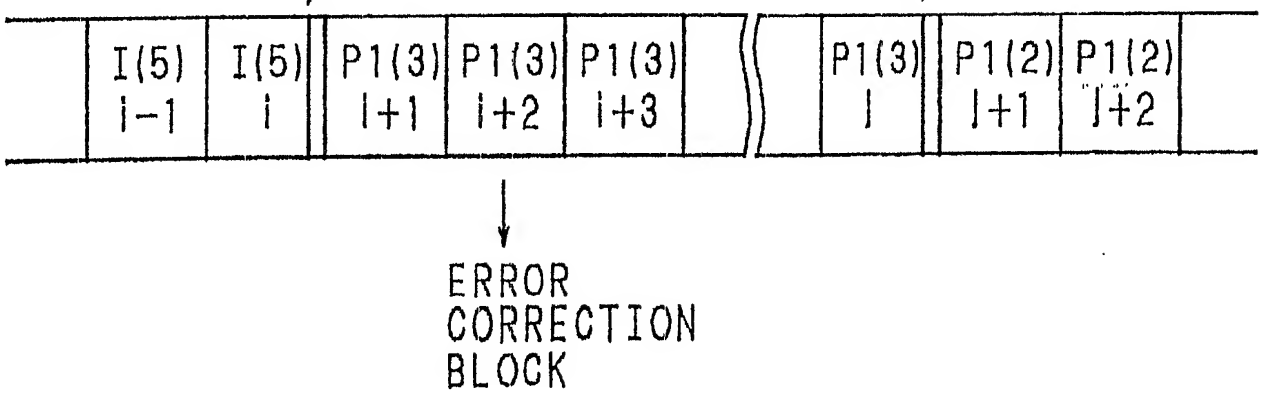


FIG. 33A

P4n(1)
P3n(2)
P2n(3)
P1n(4)
In (5)

FIG. 33B

In+1(1)
P4n (2)
P3n (3)
P2n (4)
P1n (5)

FIG. 33C

P1n+1(1)
In+1 (2)
P4n (3)
P3n (4)
P2n (5)

FIG. 33D

P2n+1(1)
P1n+1(2)
In+1 (3)
P4n (4)
P5n+1(5)

FIG. 33E

P3n+1(1)
P2n+1(2)
P1n+1(3)
In+1 (4)
P4n (5)

FIG. 33F

P4n+1(1)
P3n+1(2)
P2n+1(3)
P1n+1(4)
In+1 (5)

FIG. 33G

In+2 (1)
P4n+1(2)
P3n+1(3)
P2n+1(4)
P1n+1(5)

FIG. 34A

P3n (1)
P2n (2)
P1n (3)
In (4)
P4n-1(5)

FIG. 34B

P3n(1)
P3n(2)
P2n(3)
P1n(4)
In (5)

FIG. 34C

In+1(1)
P4n (2)
P3n (3)
P2n (4)
P1n (5)

FIG. 34D

P1n+1(1)
In+1 (2)
P4n (3)
P3n (4)
P2n (5)

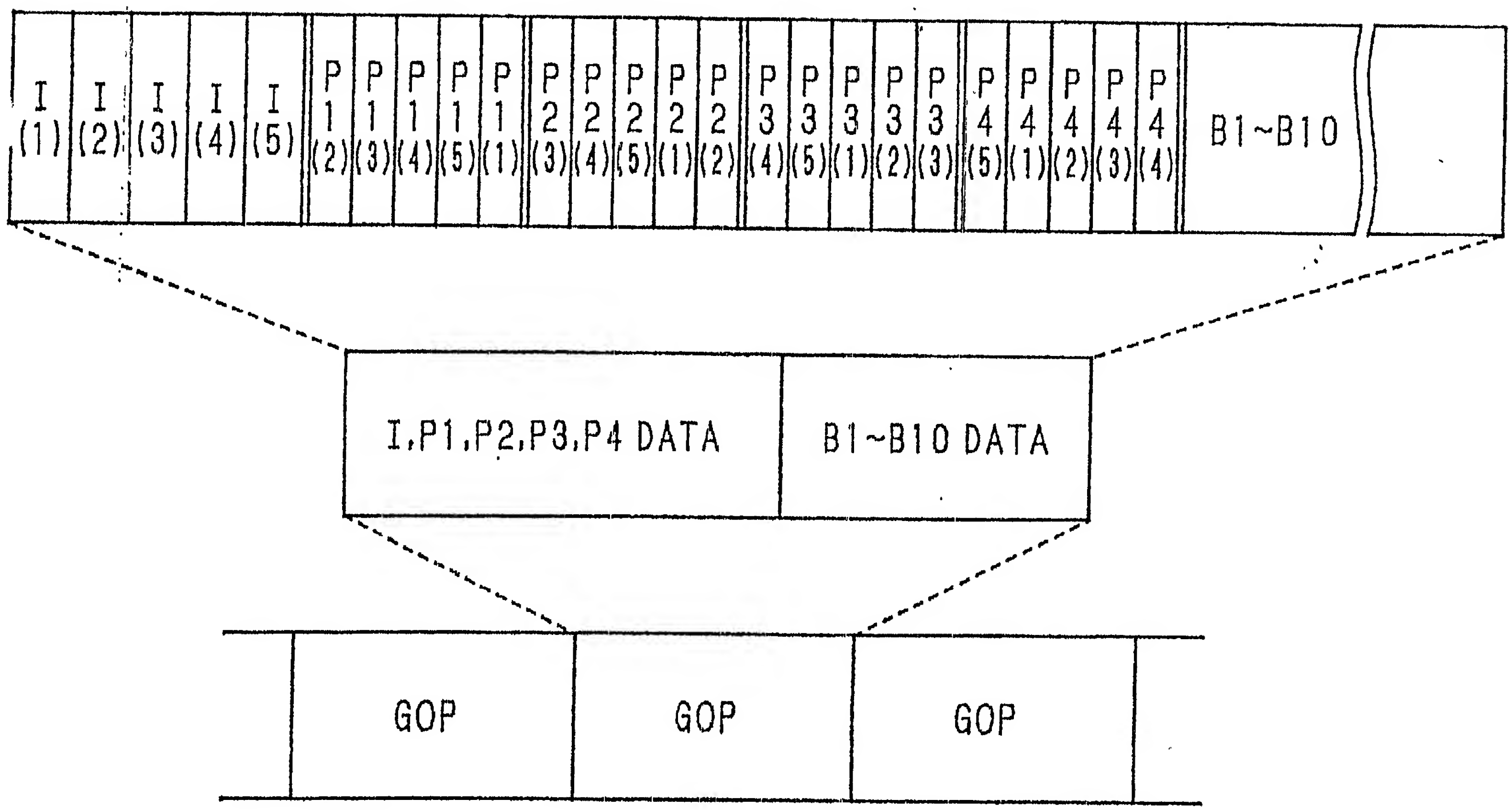
FIG. 34E

P2n+1(1)
P1n+1(2)
In+1 (3)
P3n (4)
P3n (5)

FIG. 34F

P3n+1(1)
P2n+1(2)
P1n+1(3)
In+1 (4)
P3n (5)

FIG. 35



I (1)
I (2)
I (3)
I (4)
I (5)
P 1 (2)
P 1 (3)
P 1 (4)
P 1 (5)
P 1 (1)
P 2 (3)
P 2 (4)
P 2 (5)
P 2 (1)
P 2 (2)
P 3 (4)
P 3 (5)
P 3 (1)
P 3 (2)
P 3 (3)
P 4 (5)
P 4 (1)
P 4 (2)
P 4 (3)
P 4 (4)
B1~B10
I,P1,P2,P3,P4 DATA
B1~B10 DATA
GOP
GOP
GOP

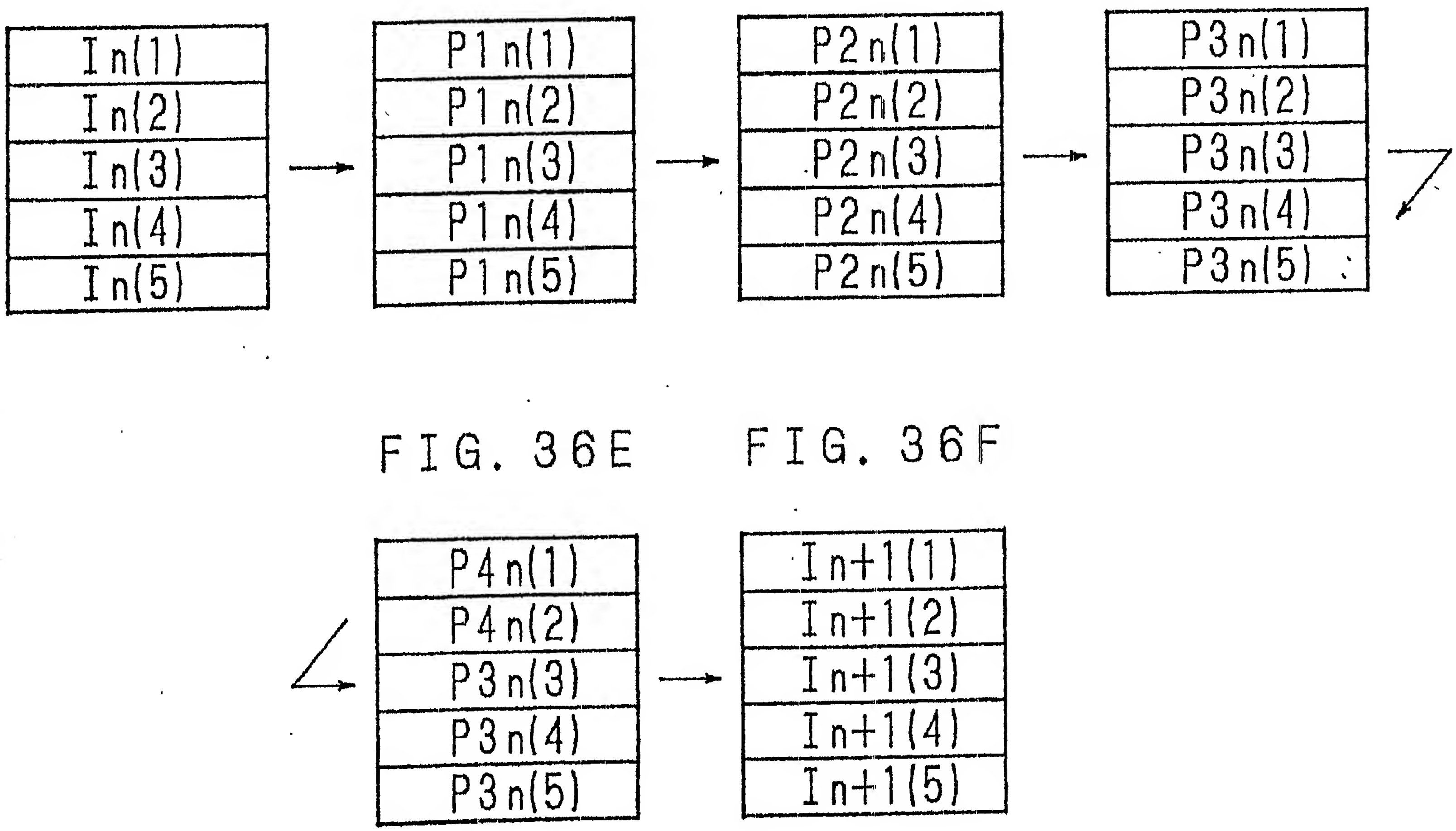


FIG. 36A

FIG. 36B

FIG. 36C

FIG. 36D

FIG. 36E

FIG. 36F

FIG. 37

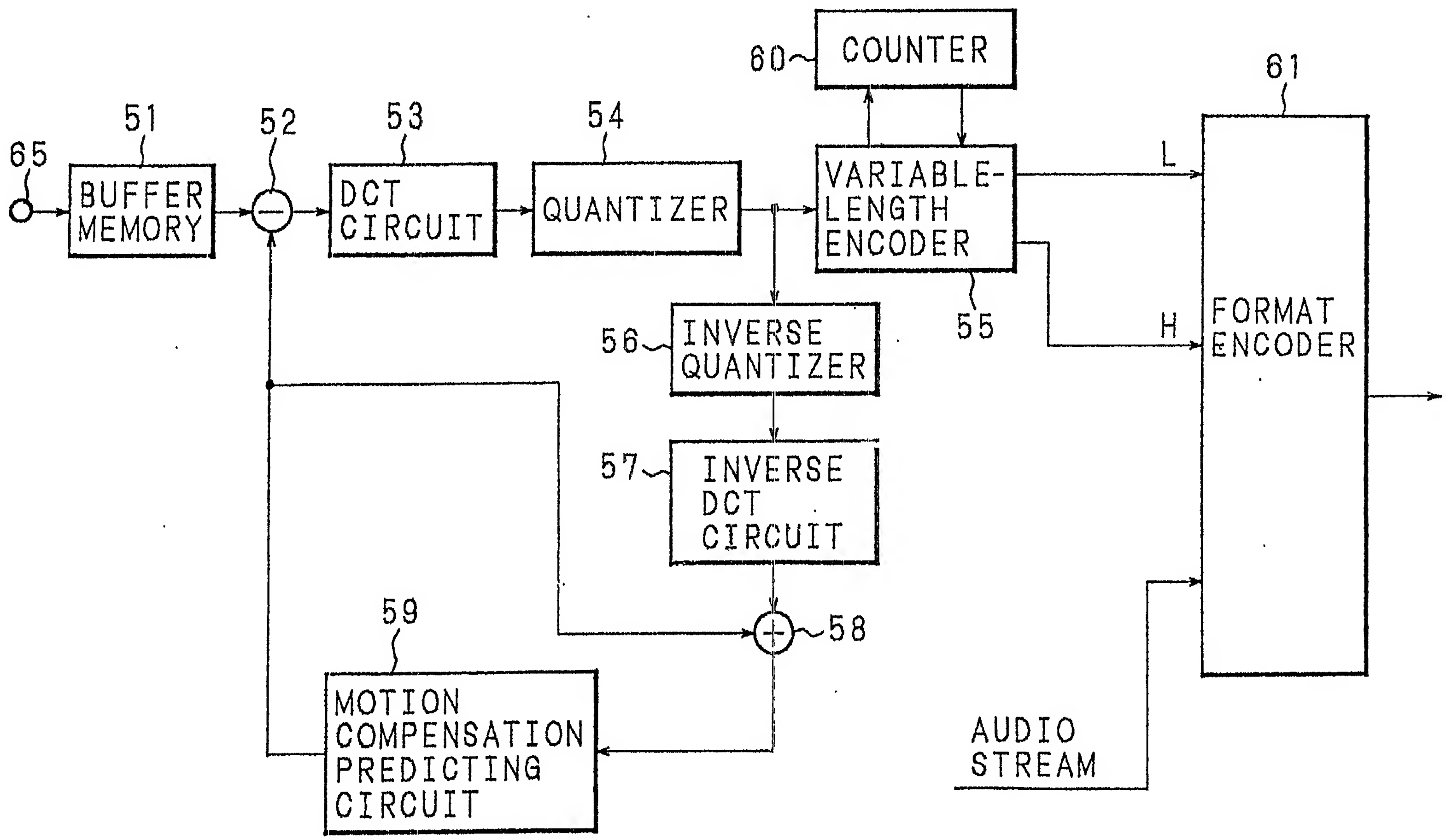

65
51
BUFFER MEMORY
52
53
DCT CIRCUIT
54
QUANTIZER
60
COUNTER
VARIABLE-LENGTH ENCODER
55
56
INVERSE QUANTIZER
57
INVERSE DCT CIRCUIT
58
59
MOTION COMPENSATION PREDICTING CIRCUIT
L
H
61
FORMAT ENCODER
AUDIO STREAM

FIG. 38

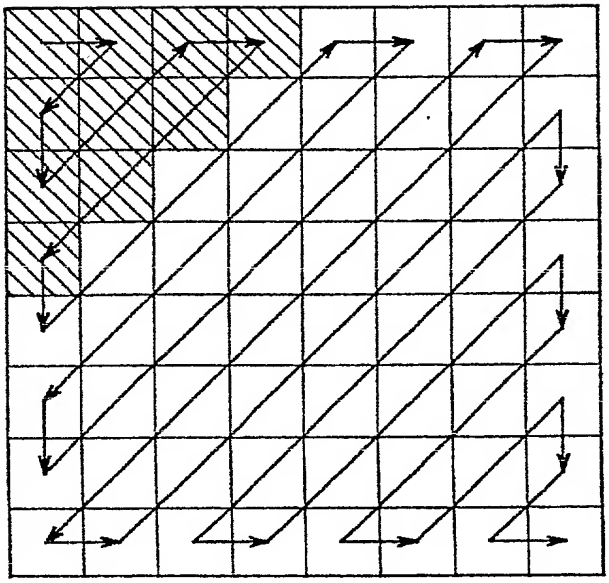


FIG. 39

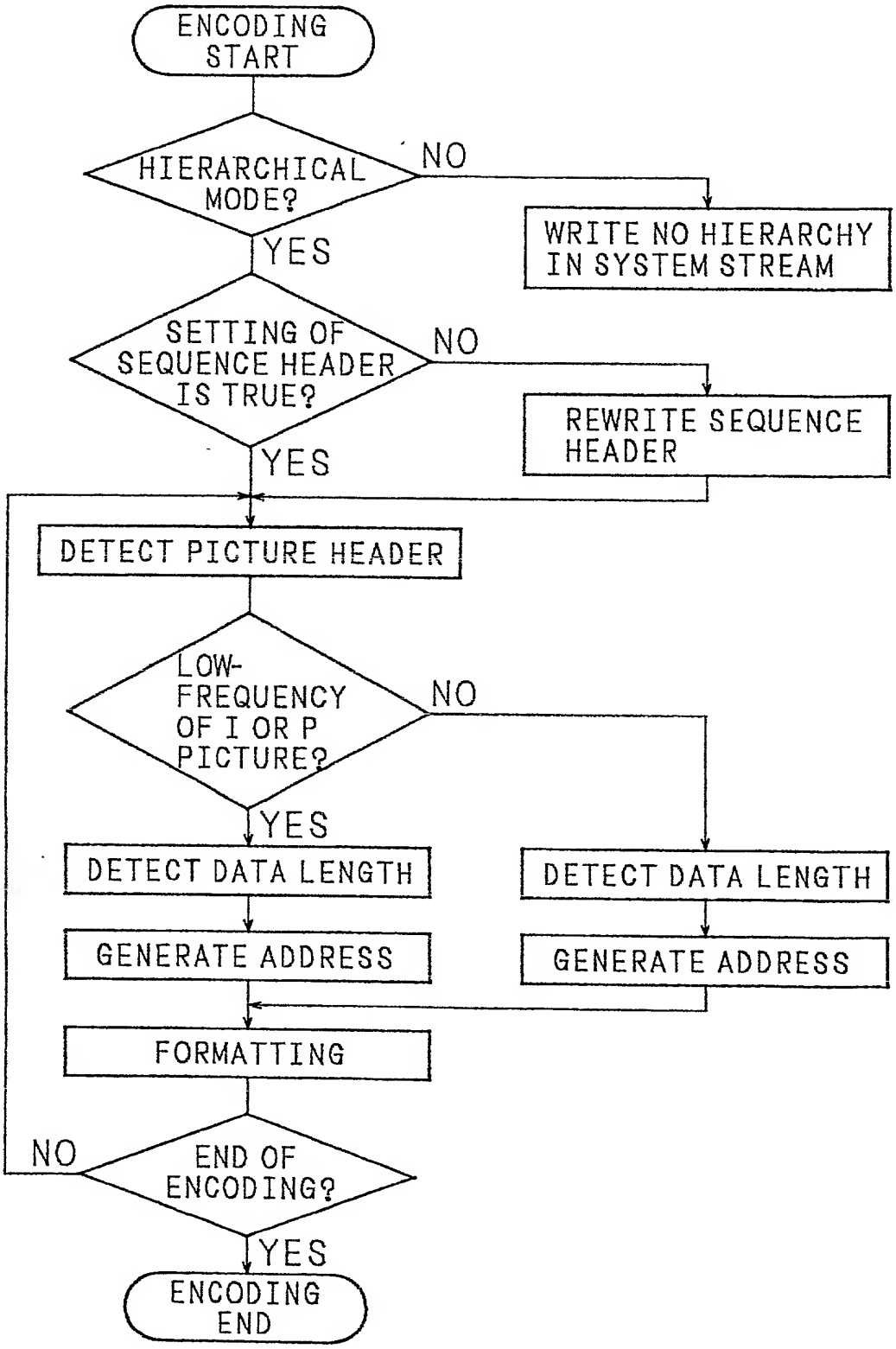

ENCODING START
HIERARCHICAL MODE?
NO
YES
WRITE NO HIERARCHY IN SYSTEM STREAM
SETTING OF SEQUENCE HEADER IS TRUE?
NO
YES
REWRITE SEQUENCE HEADER
DETECT PICTURE HEADER
LOW-FREQUENCY OF I OR P PICTURE?
NO
YES
DETECT DATA LENGTH
GENERATE ADDRESS
DETECT DATA LENGTH
GENERATE ADDRESS
FORMATTING
NO
END OF ENCODING?
YES
ENCODING END

FIG. 40

```
sequence_scalable_extension(){
    extension_start_code_identifier
    scalable_mode
    layer_id
    if(scalable_mode=="spatial scalability"){
        lower_layer_prediction_horizontal_size
        maker_bit
        lower_layer_prediction_vertical_size
        horizontal_subsampling_factor_m
        horizontal_subsampling_factor_n
        vertical_subsampling_factor_m
        vertical_subsampling_factor_n
    }
    if(scalable_mode=="temporal scalability"){
        picture_mux_enable
        if(picture_mux_enable)
            mux_to_progressive_sequence
        picture_mux_order
        picture_mux_factor
    }
    next_start_code()
}

slice(){
    slice_start_code
    if(vertical_size>2800)
        slice_vertical_position_extension
    if(<sequence_scalable_extention()is present in the bitstresm>)
        if(scalable_mode=="data partitioning")
            priority_breakpoint
    quantiser_scale_code
    if(nextbits()=='1'){
        intra_slice_flag
        intra_slice
        reserved_bits
        while(nextbits()=='1'){
            extra_bit_slice
            extra_information_slice
        }
    }
    extra_bit_slice
    do{
      macroblock()
    }while(nextbits()!='000 0000 0000 0000 0000 0000')
    next_start_code()
}
```

FIG. 41A
BITSTREAM IN NO HIERARCHY

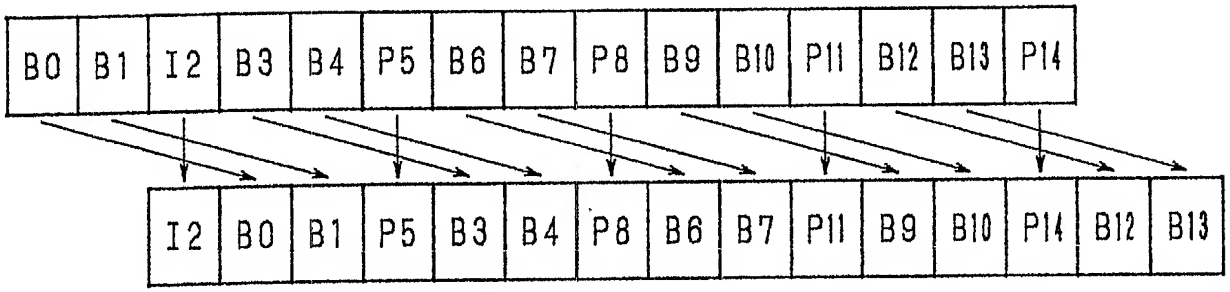


FIG. 41B
BITSTREAM IN HIERARCHY

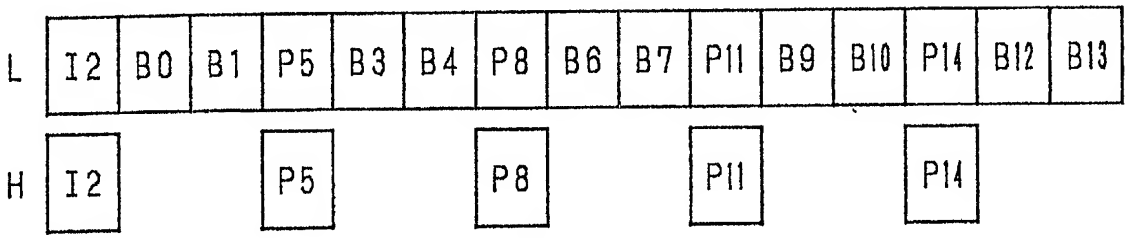


FIG. 41C
REARRANGED BITSTREAM IN CONSIDERATION OF SPECIAL PLAYBACK

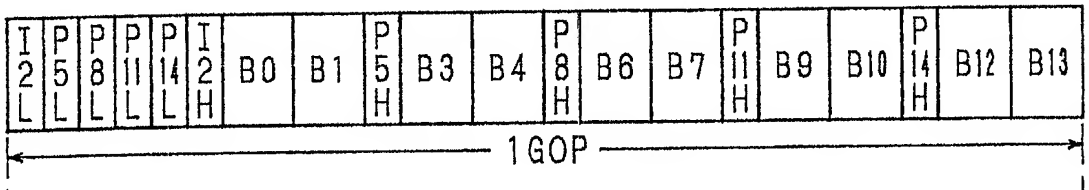


FIG. 41D
PROGRAM STREAM FOR DISC RECORDING

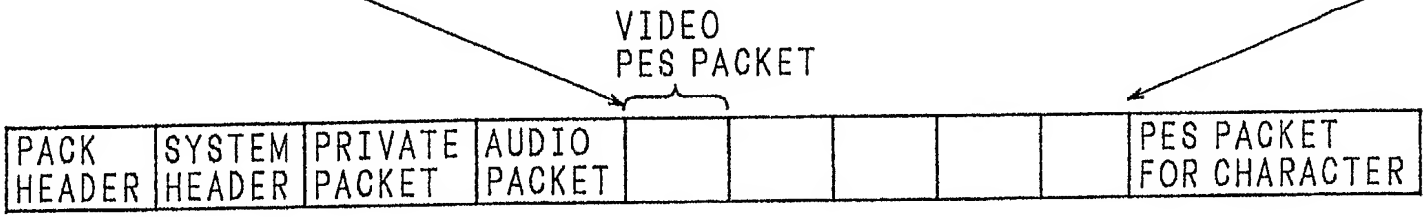


FIG. 42

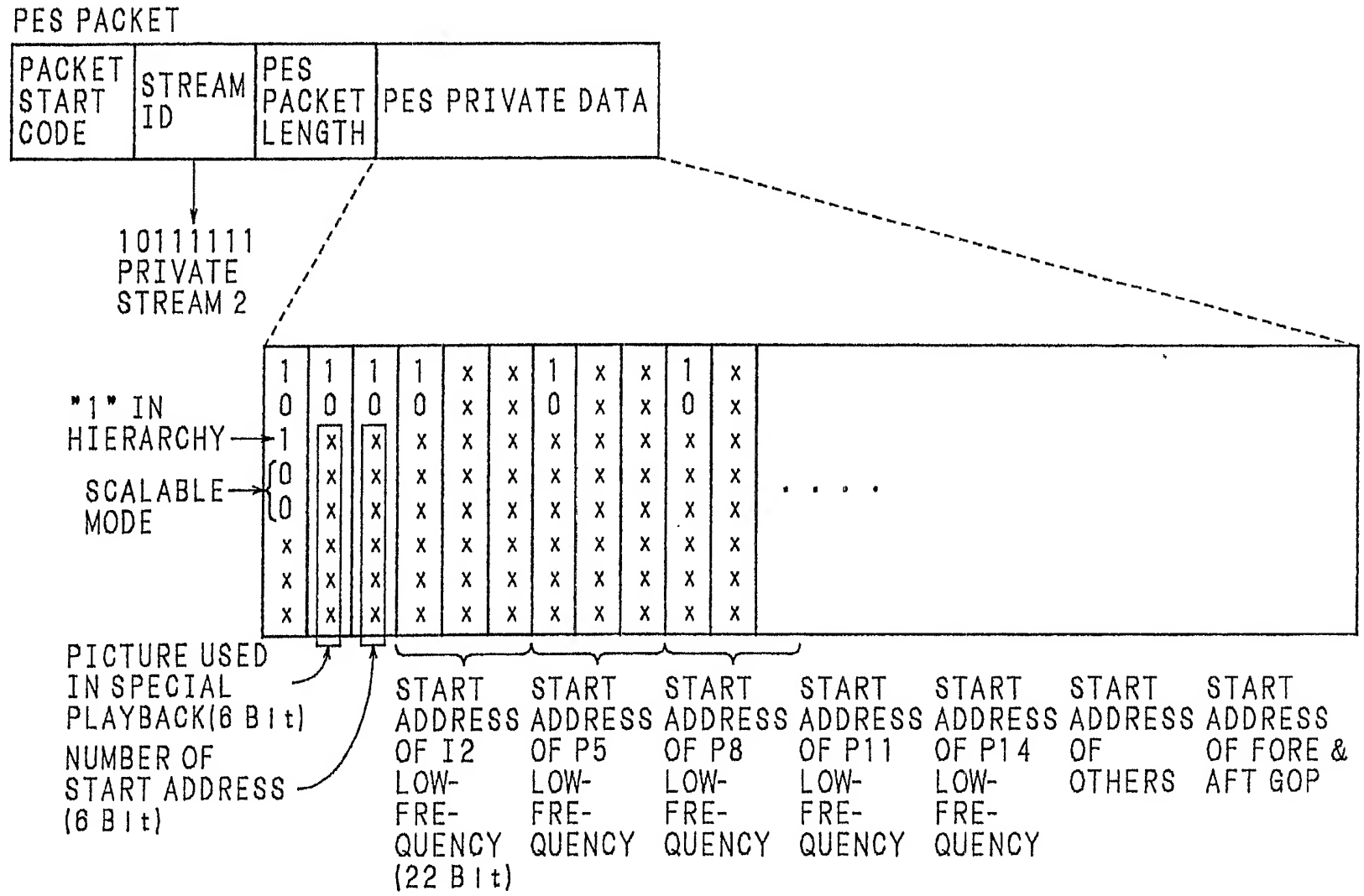

PES PACKET
PACKET START CODE
STREAM ID
PES PACKET LENGTH
PES PRIVATE DATA
10111111
PRIVATE STREAM 2
"1" IN HIERARCHY
SCALABLE MODE
PICTURE USED IN SPECIAL PLAYBACK(6 Bit)
NUMBER OF START ADDRESS (6 Bit)
START ADDRESS OF I2 LOW-FRE-QUENCY (22 Bit)
START ADDRESS OF P5 LOW-FRE-QUENCY
START ADDRESS OF P8 LOW-FRE-QUENCY
START ADDRESS OF P11 LOW-FRE-QUENCY
START ADDRESS OF P14 LOW-FRE-QUENCY
START ADDRESS OF OTHERS
START ADDRESS OF FORE & AFT GOP

FIG. 43

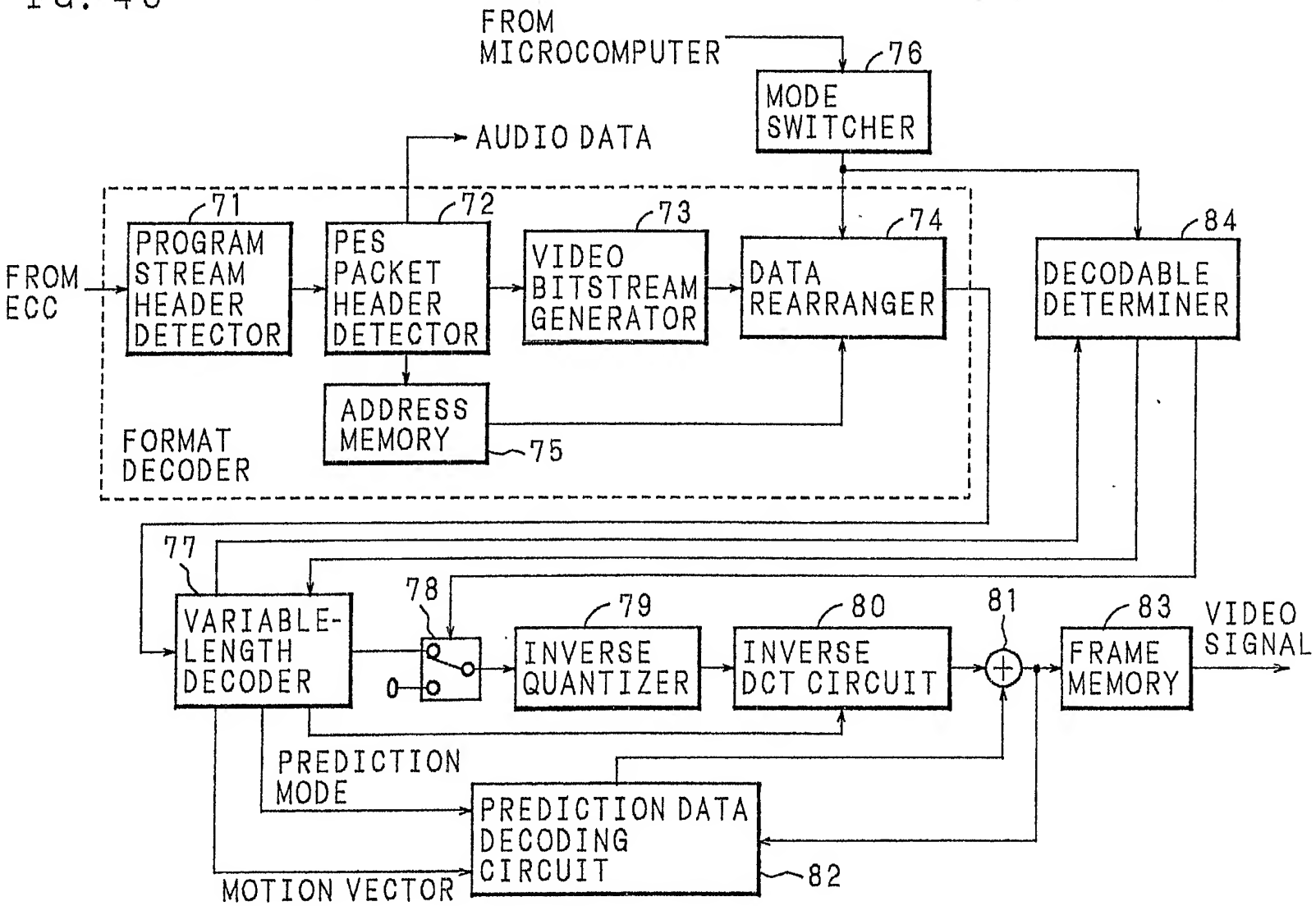

FROM MICROCOMPUTER
76
MODE SWITCHER
AUDIO DATA
71
72
73
74
84
FROM ECC
PROGRAM STREAM HEADER DETECTOR
PES PACKET HEADER DETECTOR
VIDEO BITSTREAM GENERATOR
DATA REARRANGER
DECODABLE DETERMINER
ADDRESS MEMORY
75
FORMAT DECODER
77
78
79
80
81
83
VIDEO SIGNAL
VARIABLE-LENGTH DECODER
INVERSE QUANTIZER
INVERSE DCT CIRCUIT
FRAME MEMORY
0
PREDICTION MODE
PREDICTION DATA DECODING CIRCUIT
82
MOTION VECTOR

FIG. 44

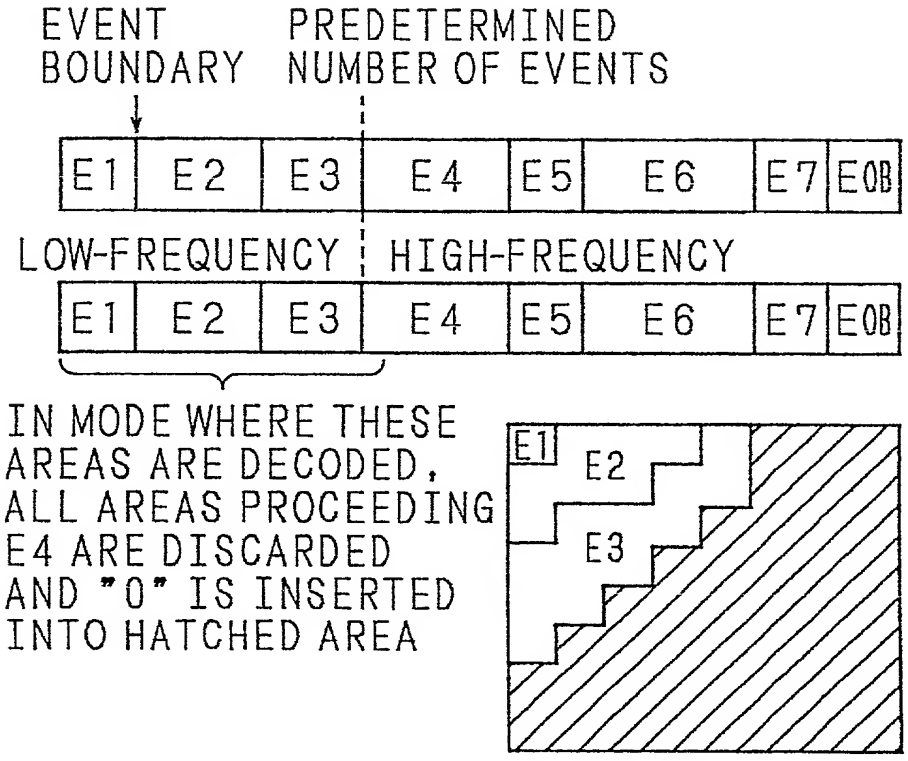

EVENT BOUNDARY
PREDETERMINED NUMBER OF EVENTS
E1
E2
E3
E4
E5
E6
E7
EOB
LOW-FREQUENCY
HIGH-FREQUENCY
E1
E2
E3
E4
E5
E6
E7
EOB
IN MODE WHERE THESE AREAS ARE DECODED, ALL AREAS PROCEEDING E4 ARE DISCARDED AND "0" IS INSERTED INTO HATCHED AREA
E1
E2
E3

FIG. 45

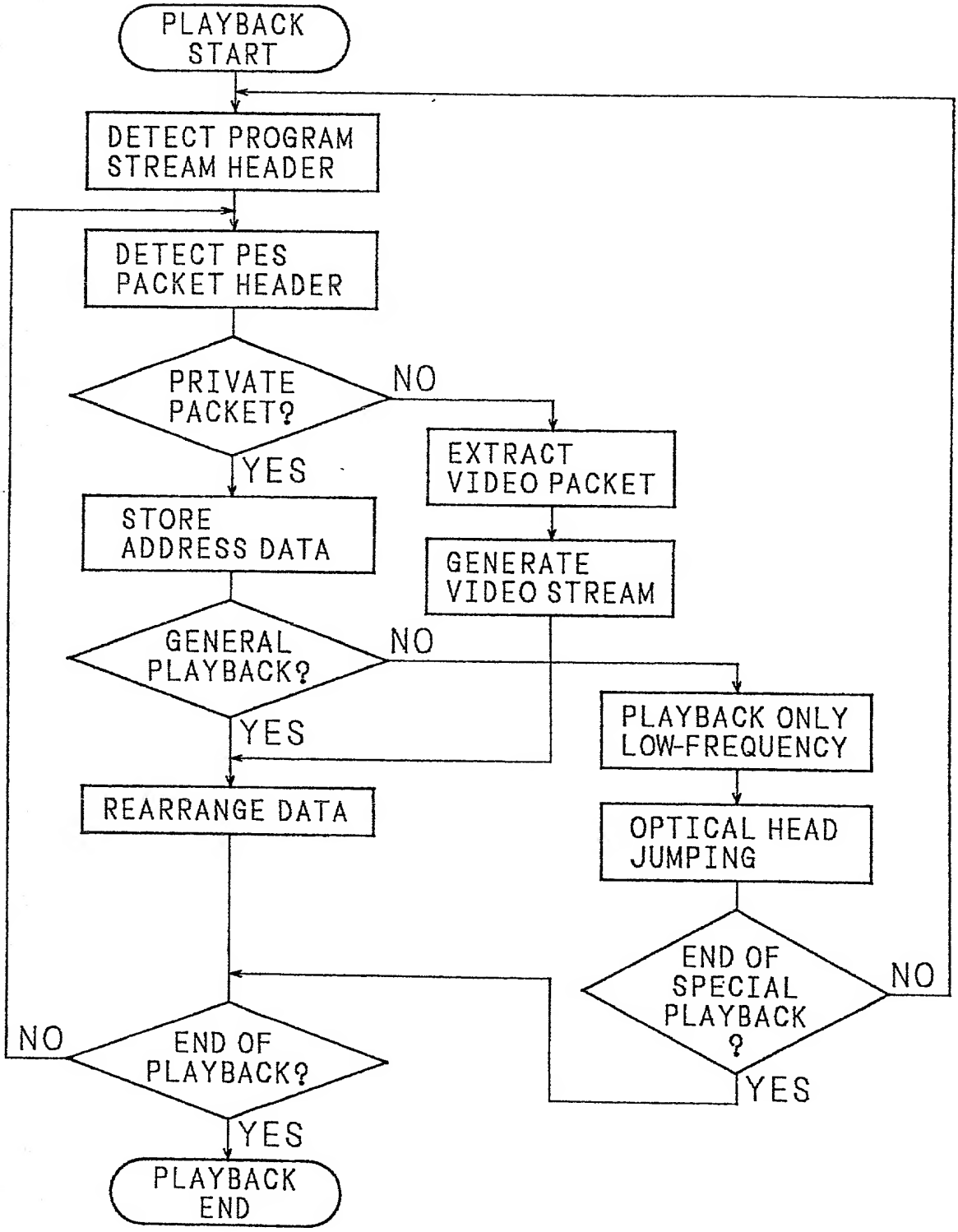

PLAYBACK START
DETECT PROGRAM STREAM HEADER
DETECT PES PACKET HEADER
PRIVATE PACKET?
NO
YES
EXTRACT VIDEO PACKET
STORE ADDRESS DATA
GENERATE VIDEO STREAM
GENERAL PLAYBACK?
NO
YES
PLAYBACK ONLY LOW-FREQUENCY
REARRANGE DATA
OPTICAL HEAD JUMPING
END OF SPECIAL PLAYBACK ?
NO
YES
NO
END OF PLAYBACK?
YES
PLAYBACK END

FIG. 46

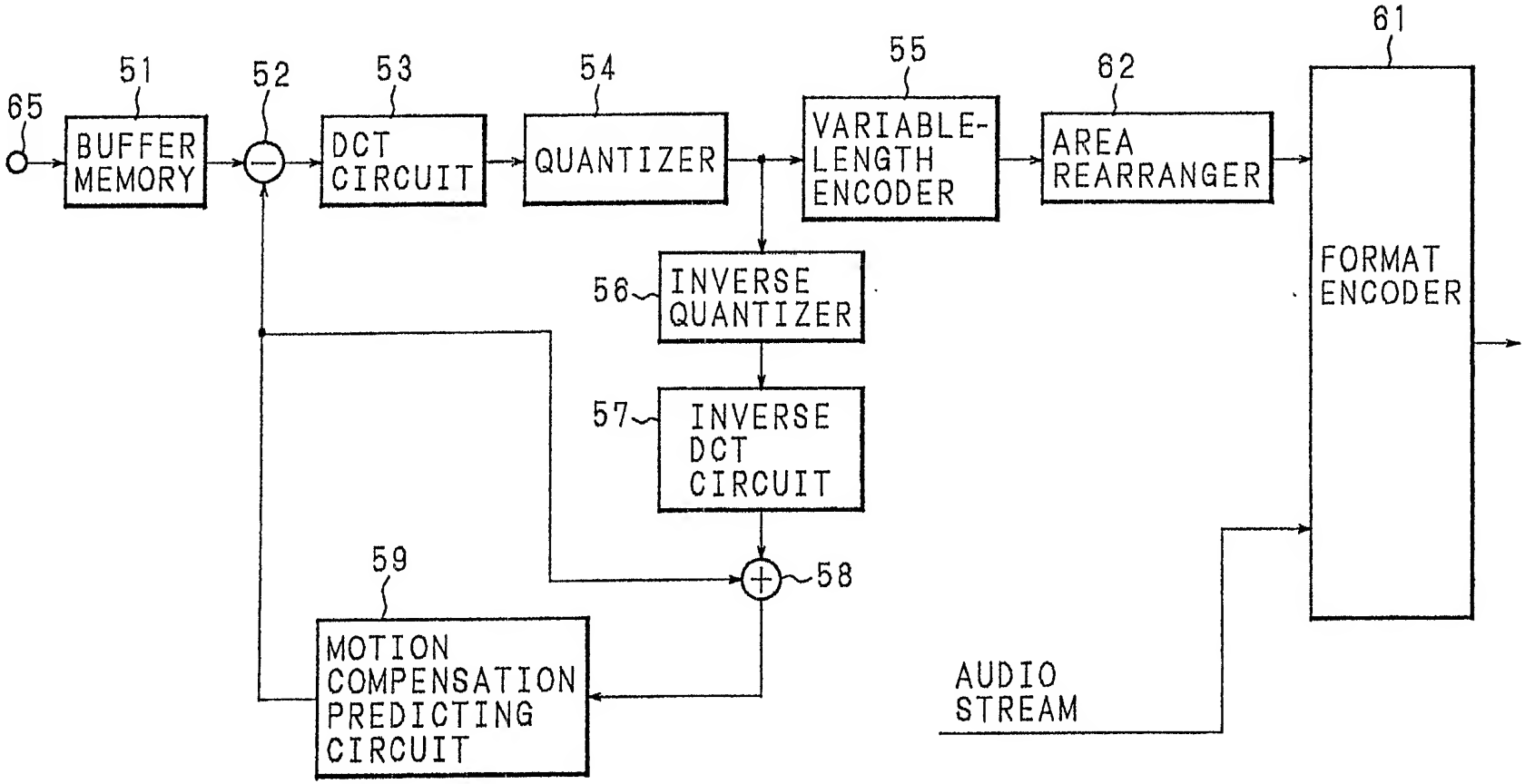

65
51
BUFFER MEMORY
52
53
DCT CIRCUIT
54
QUANTIZER
55
VARIABLE-LENGTH ENCODER
62
AREA REARRANGER
61
FORMAT ENCODER
56
INVERSE QUANTIZER
57
INVERSE DCT CIRCUIT
58
59
MOTION COMPENSATION PREDICTING CIRCUIT
AUDIO STREAM

FIG. 47

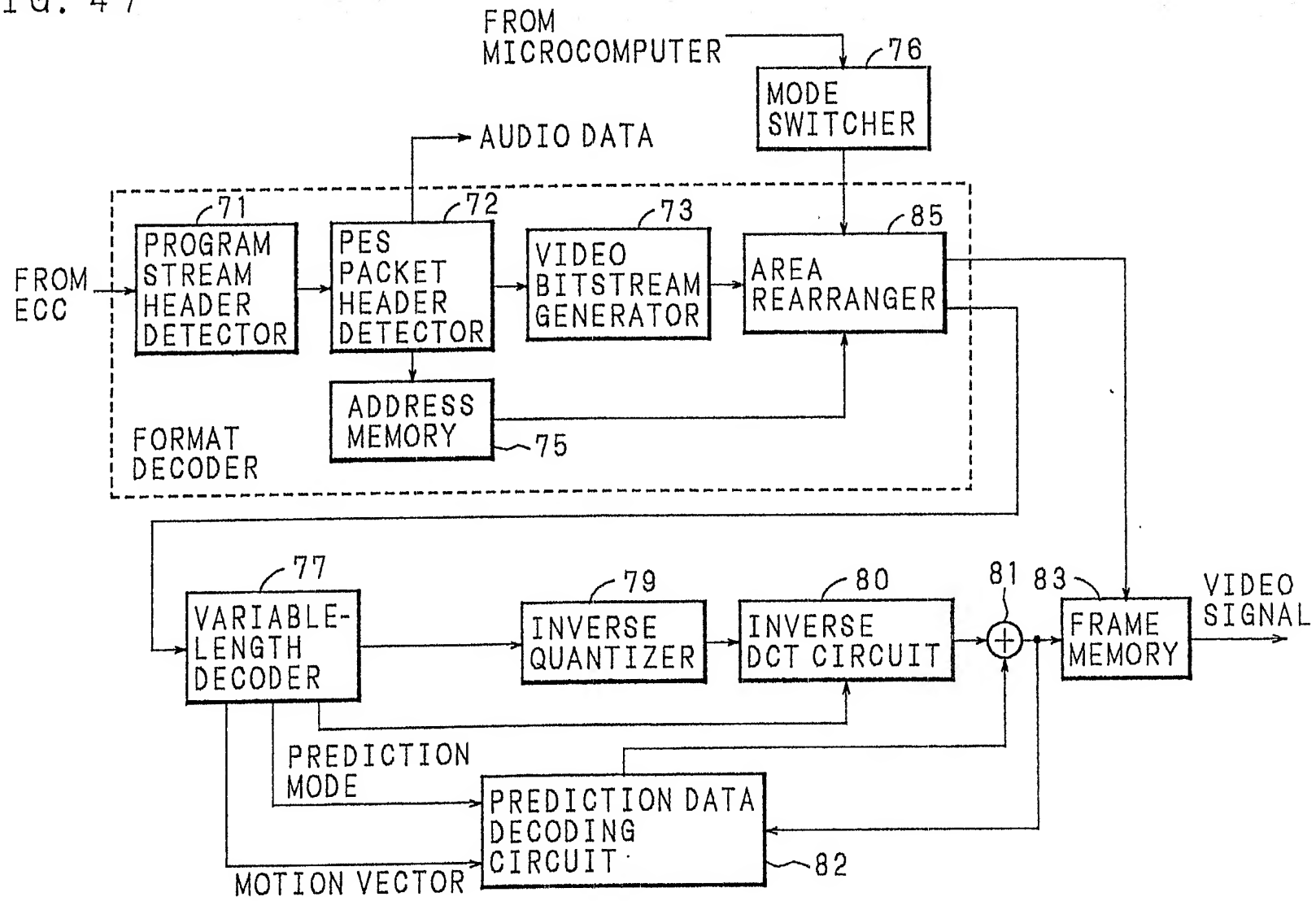

FROM MICROCOMPUTER
76
MODE SWITCHER
AUDIO DATA
71
72
73
85
FROM ECC
PROGRAM STREAM HEADER DETECTOR
PES PACKET HEADER DETECTOR
VIDEO BITSTREAM GENERATOR
AREA REARRANGER
ADDRESS MEMORY
75
FORMAT DECODER
77
79
80
81
83
VIDEO SIGNAL
VARIABLE-LENGTH DECODER
INVERSE QUANTIZER
INVERSE DCT CIRCUIT
FRAME MEMORY
PREDICTION MODE
PREDICTION DATA DECODING CIRCUIT
82
MOTION VECTOR

FIG. 48

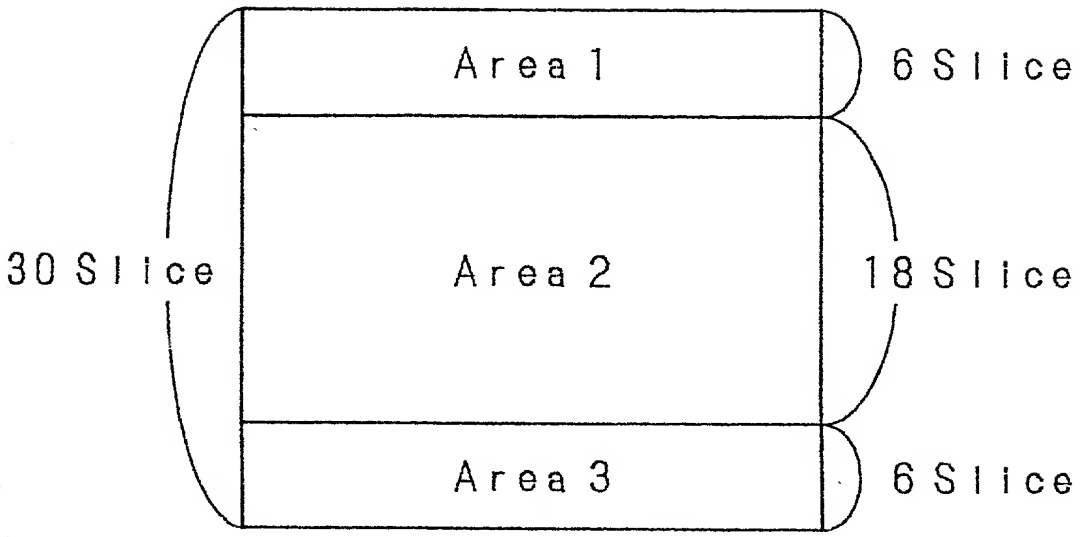


FIG. 49

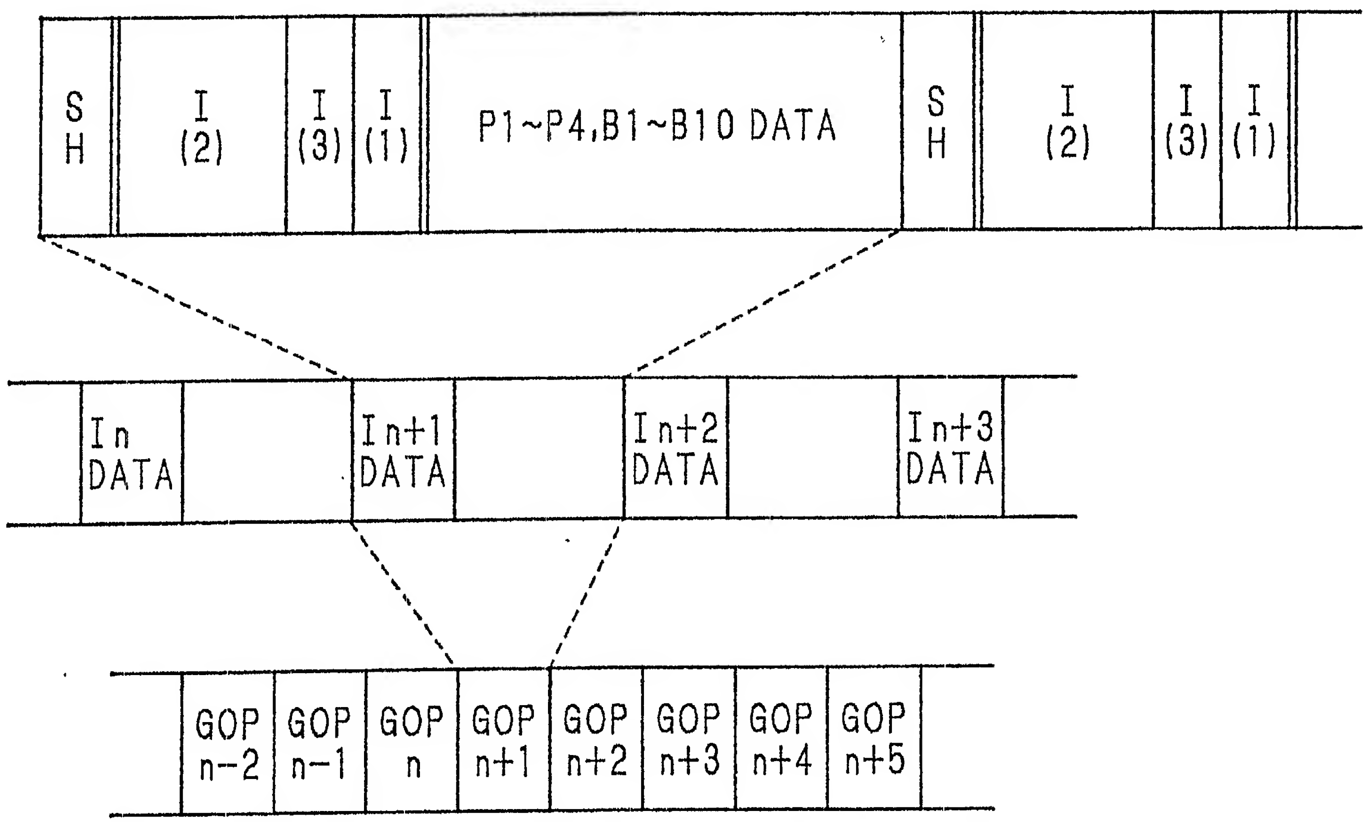

S H
I (2)
I (3)
I (1)
P1~P4,B1~B10 DATA
S H
I (2)
I (3)
I (1)
In DATA
In+1 DATA
In+2 DATA
In+3 DATA
GOP n-2
GOP n-1
GOP n
GOP n+1
GOP n+2
GOP n+3
GOP n+4
GOP n+5

FIG. 50

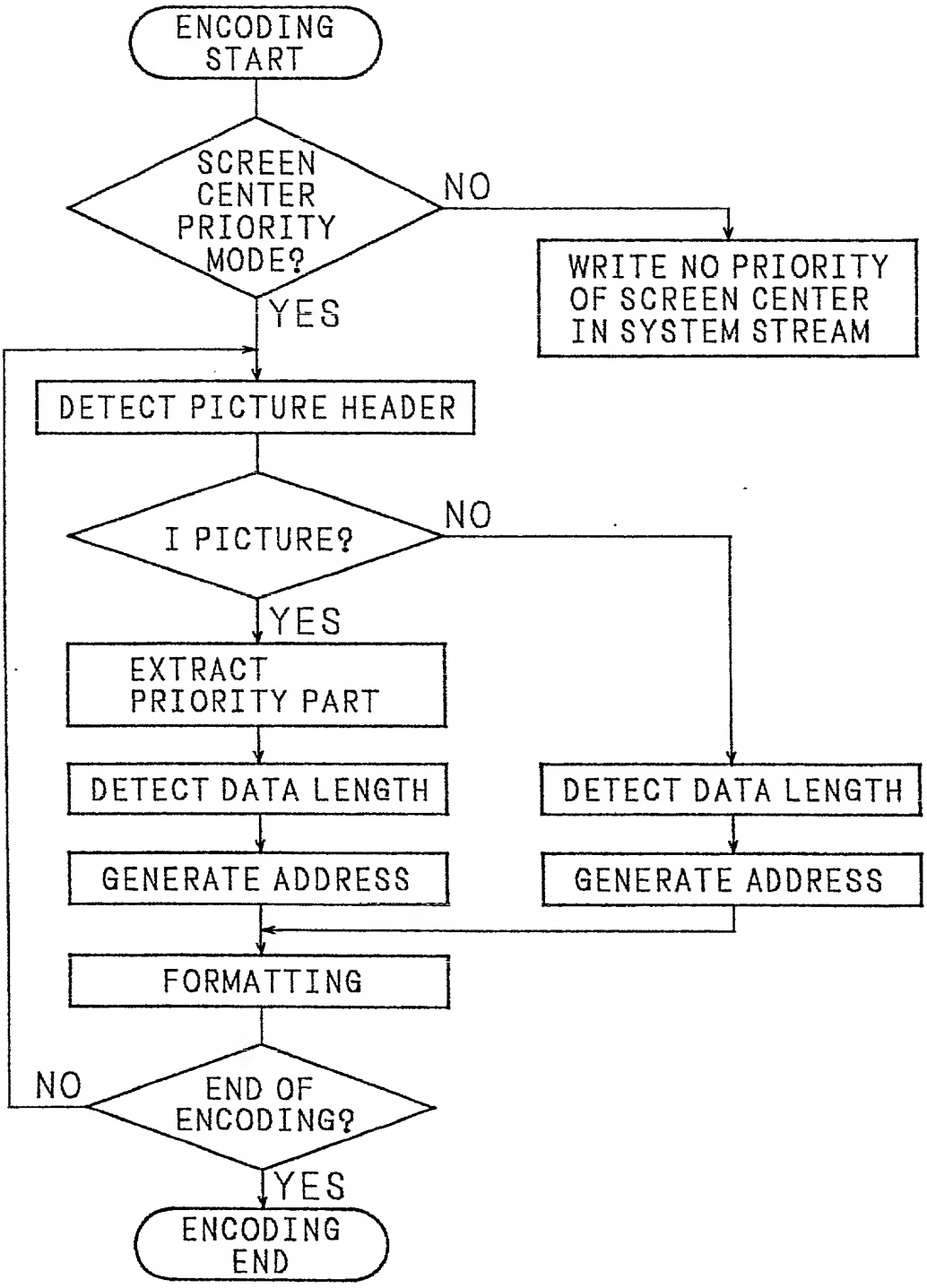

ENCODING START
SCREEN CENTER PRIORITY MODE?
NO
YES
WRITE NO PRIORITY OF SCREEN CENTER IN SYSTEM STREAM
DETECT PICTURE HEADER
I PICTURE?
NO
YES
EXTRACT PRIORITY PART
DETECT DATA LENGTH
GENERATE ADDRESS
DETECT DATA LENGTH
GENERATE ADDRESS
FORMATTING
NO
END OF ENCODING?
YES
ENCODING END

FIG. 51

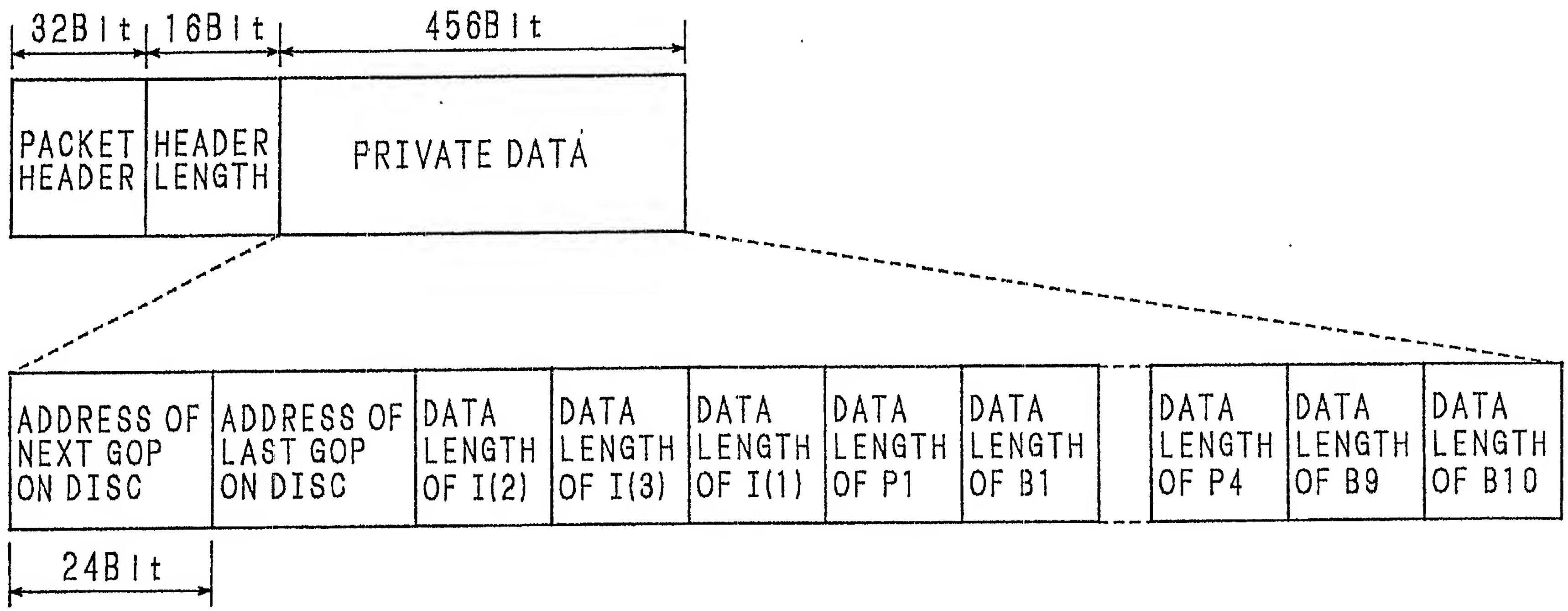

32Bit
16Bit
456Bit
PACKET HEADER
HEADER LENGTH
PRIVATE DATA
ADDRESS OF NEXT GOP ON DISC
ADDRESS OF LAST GOP ON DISC
DATA LENGTH OF I(2)
DATA LENGTH OF I(3)
DATA LENGTH OF I(1)
DATA LENGTH OF P1
DATA LENGTH OF B1
DATA LENGTH OF P4
DATA LENGTH OF B9
DATA LENGTH OF B10
24Bit

FIG. 52

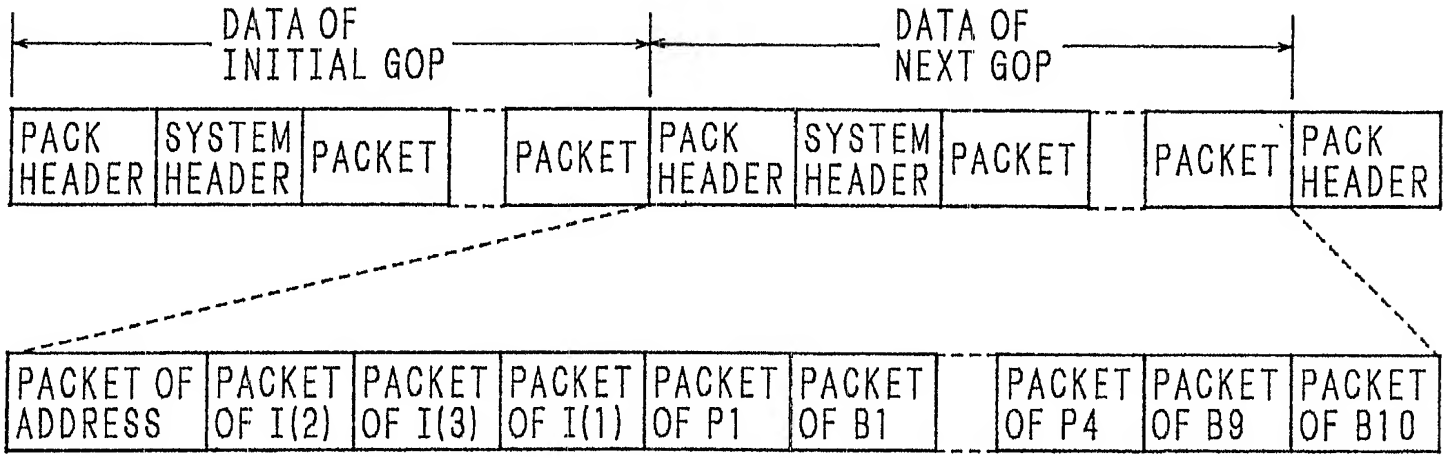

DATA OF INITIAL GOP
DATA OF NEXT GOP
PACK HEADER
SYSTEM HEADER
PACKET
PACKET
PACK HEADER
SYSTEM HEADER
PACKET
PACKET
PACK HEADER
PACKET OF ADDRESS
PACKET OF I(2)
PACKET OF I(3)
PACKET OF I(1)
PACKET OF P1
PACKET OF B1
PACKET OF P4
PACKET OF B9
PACKET OF B10

FIG. 53A FIG. 53B FIG. 53C FIG. 53D FIG. 53E

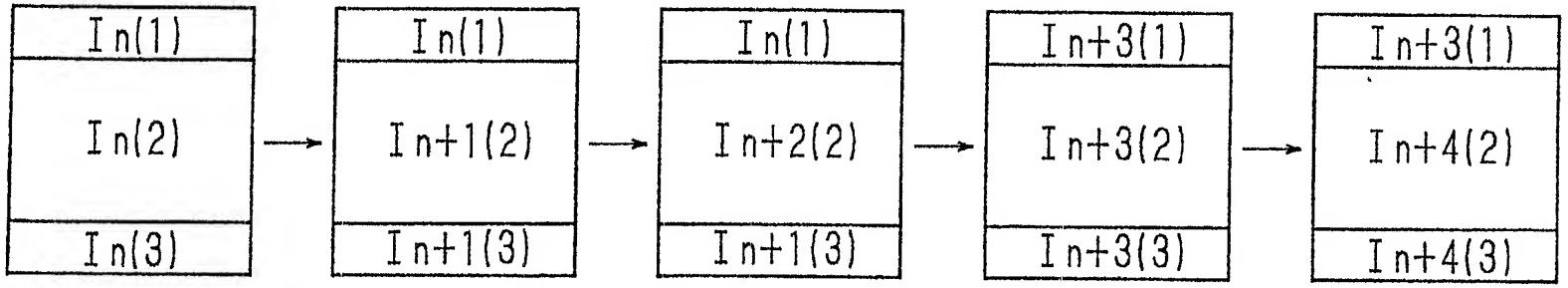


FIG. 54A FIG. 54B FIG. 54C FIG. 54D FIG. 54E

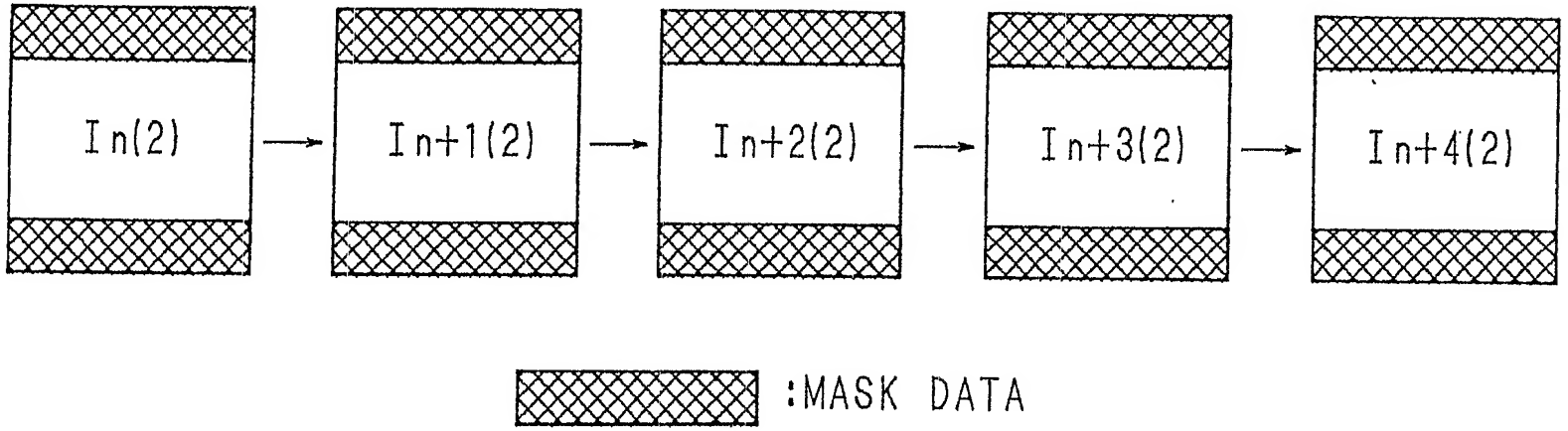


FIG. 55A

FIG. 55B

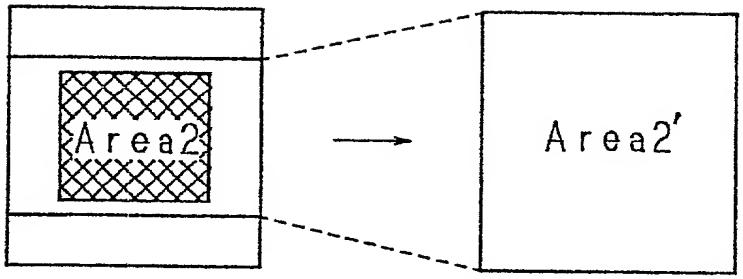


FIG. 56

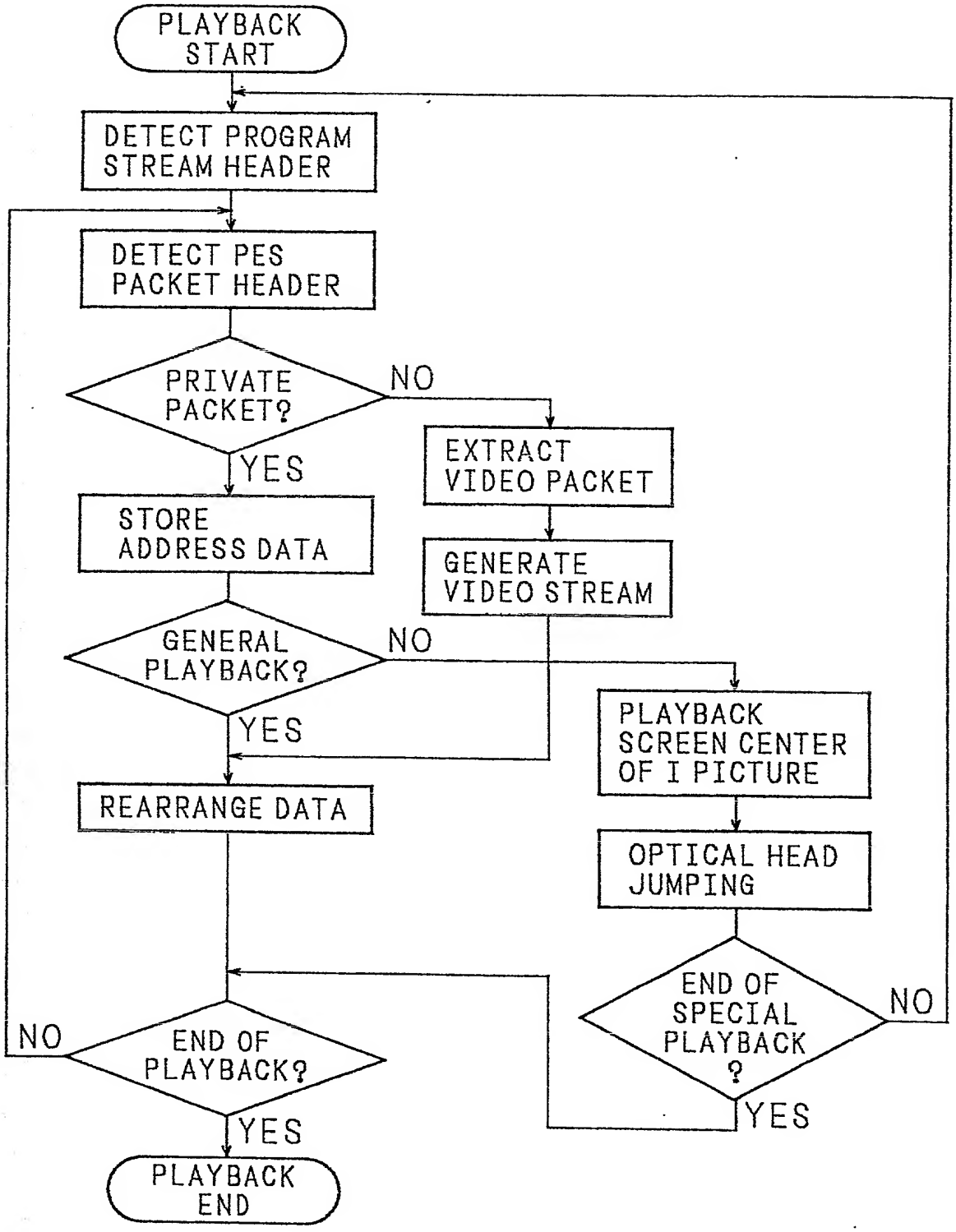

PLAYBACK START
DETECT PROGRAM STREAM HEADER
DETECT PES PACKET HEADER
PRIVATE PACKET?
NO
YES
EXTRACT VIDEO PACKET
STORE ADDRESS DATA
GENERATE VIDEO STREAM
GENERAL PLAYBACK?
NO
YES
PLAYBACK SCREEN CENTER OF I PICTURE
REARRANGE DATA
OPTICAL HEAD JUMPING
END OF SPECIAL PLAYBACK ?
NO
YES
NO
END OF PLAYBACK?
YES
PLAYBACK END

FIG. 57

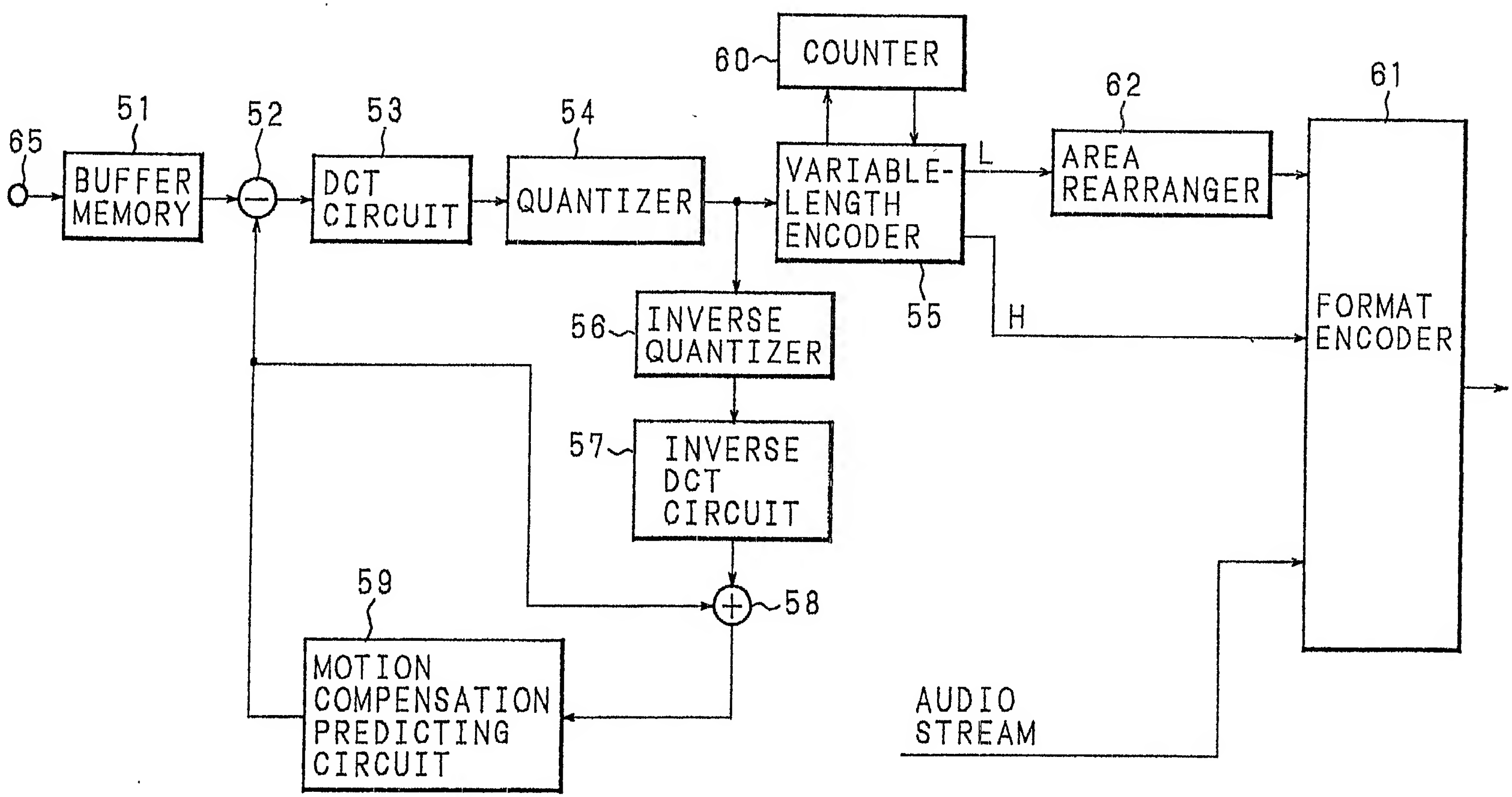

65
51
BUFFER MEMORY
52
53
DCT CIRCUIT
54
QUANTIZER
60
COUNTER
VARIABLE-LENGTH ENCODER
55
L
H
62
AREA REARRANGER
61
FORMAT ENCODER
56
INVERSE QUANTIZER
57
INVERSE DCT CIRCUIT
58
59
MOTION COMPENSATION PREDICTING CIRCUIT
AUDIO STREAM

FIG. 58

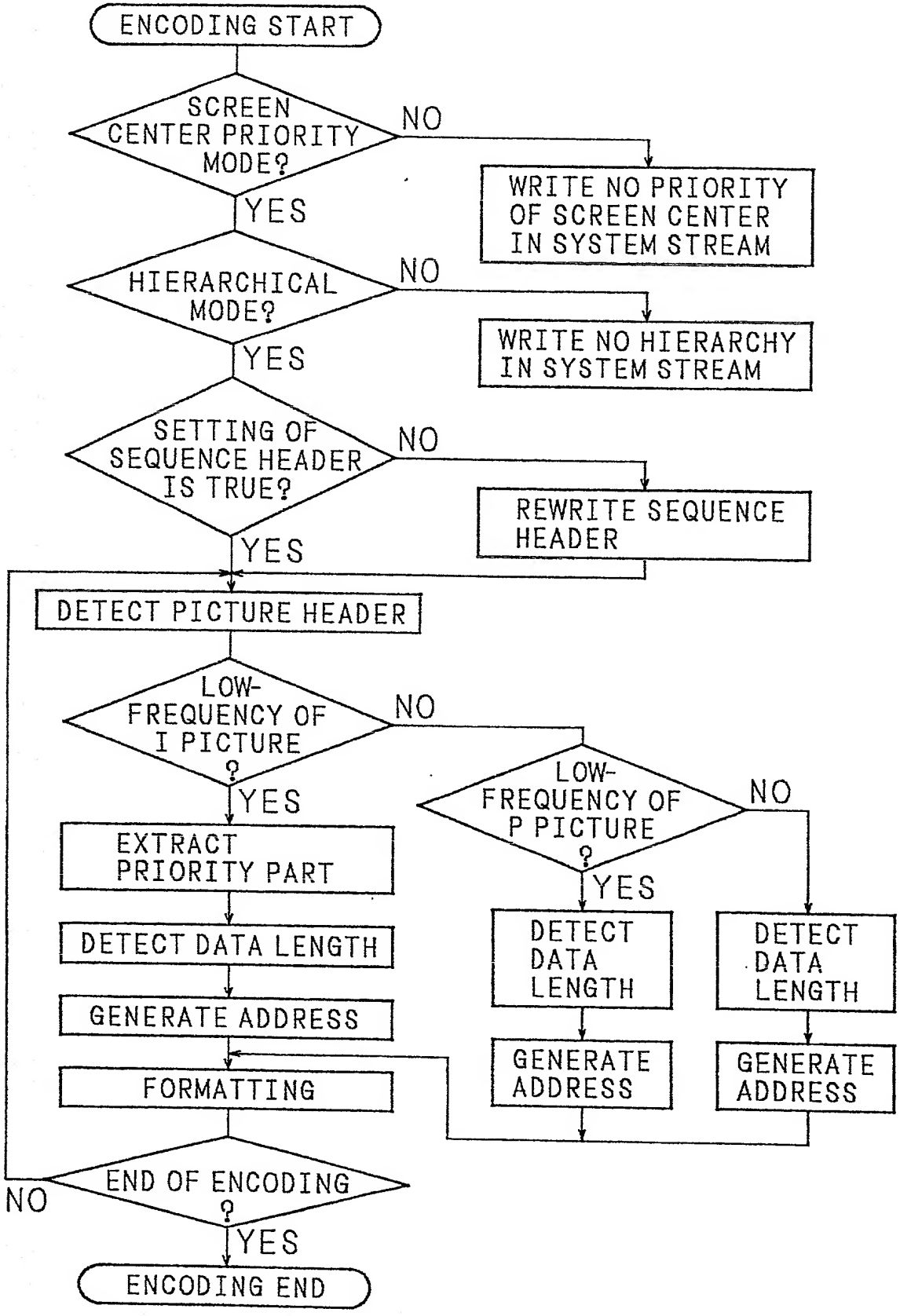

ENCODING START
SCREEN CENTER PRIORITY MODE?
NO
YES
WRITE NO PRIORITY OF SCREEN CENTER IN SYSTEM STREAM
HIERARCHICAL MODE?
NO
YES
WRITE NO HIERARCHY IN SYSTEM STREAM
SETTING OF SEQUENCE HEADER IS TRUE?
NO
YES
REWRITE SEQUENCE HEADER
DETECT PICTURE HEADER
LOW-FREQUENCY OF I PICTURE ?
NO
YES
EXTRACT PRIORITY PART
DETECT DATA LENGTH
GENERATE ADDRESS
FORMATTING
LOW-FREQUENCY OF P PICTURE ?
NO
YES
DETECT DATA LENGTH
GENERATE ADDRESS
DETECT DATA LENGTH
GENERATE ADDRESS
END OF ENCODING ?
NO
YES
ENCODING END

FIG. 59A
BITSTREAM IN NO HIERARCHY

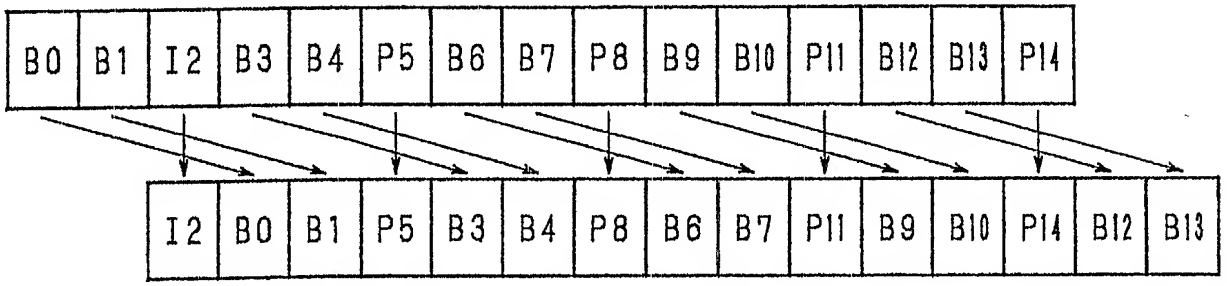


FIG. 59B
BITSTREAM IN HIERARCHY

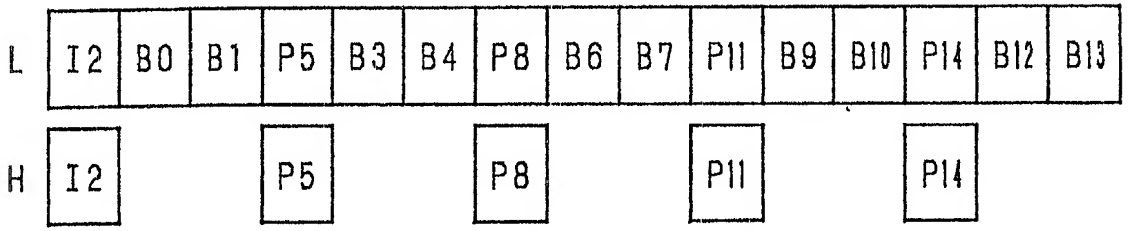


FIG. 59C
REARRANGED BITSTREAM IN CONSIDERATION OF SPECIAL PLAYBACK

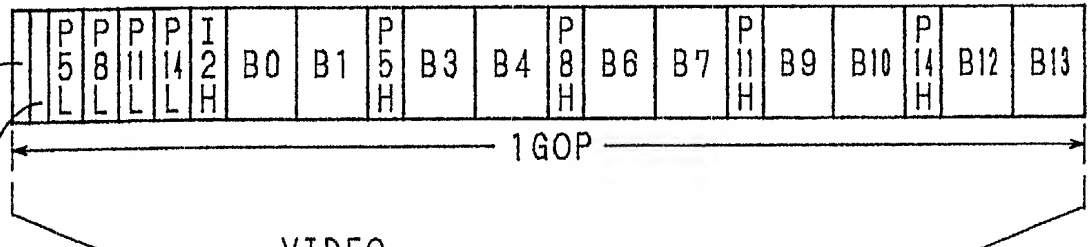


FIG. 59D
PROGRAM STREAM FOR DISC RECORDING

FIG. 60

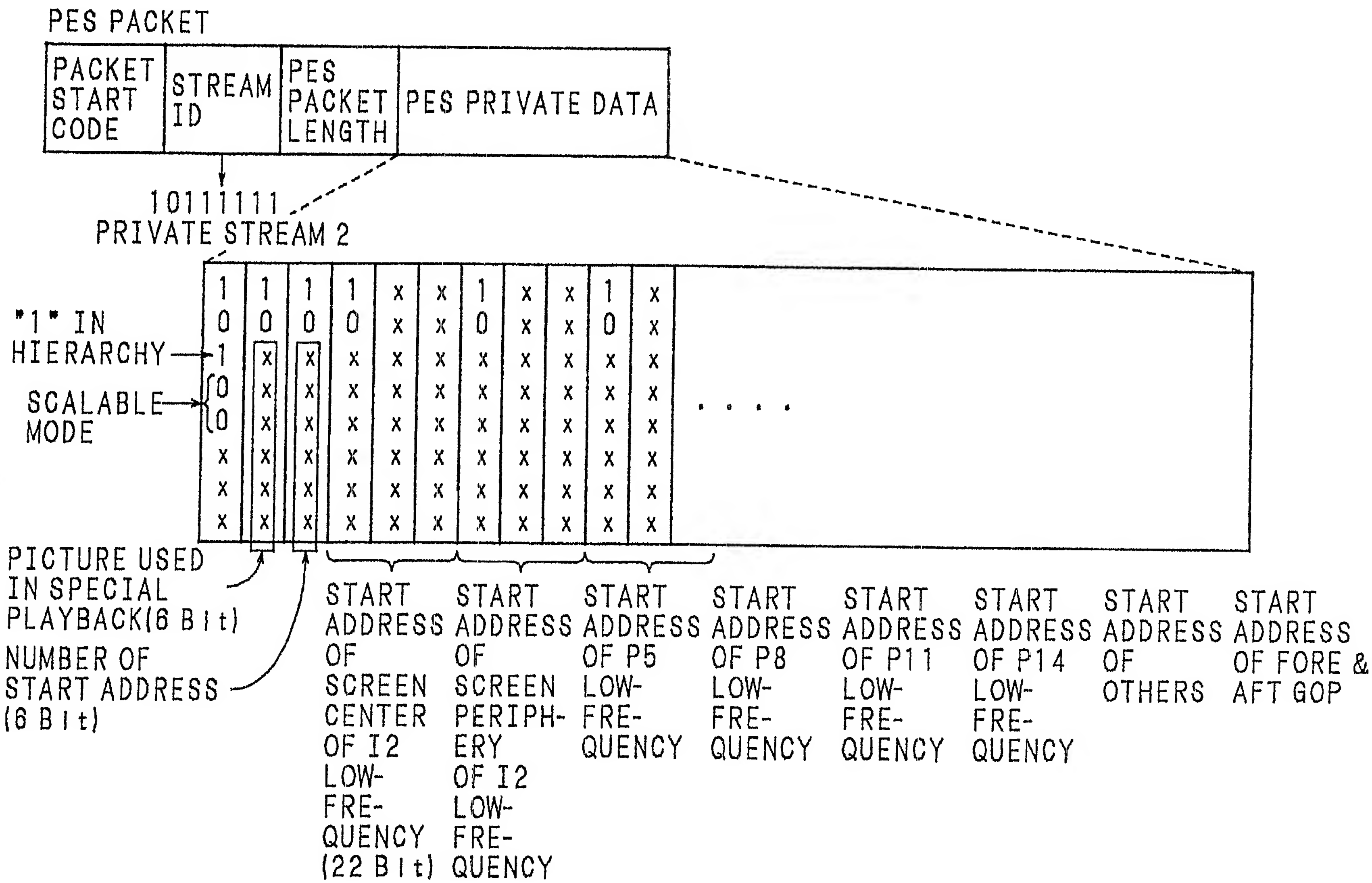

PES PACKET
PACKET START CODE
STREAM ID
PES PACKET LENGTH
PES PRIVATE DATA
10111111
PRIVATE STREAM 2
"1" IN HIERARCHY
SCALABLE MODE
PICTURE USED IN SPECIAL PLAYBACK(6 Bit)
NUMBER OF START ADDRESS (6 Bit)
START ADDRESS OF SCREEN CENTER OF I2 LOW-FRE-QUENCY (22 Bit)
START ADDRESS OF SCREEN PERIPH-ERY OF I2 LOW-FRE-QUENCY
START ADDRESS OF P5 LOW-FRE-QUENCY
START ADDRESS OF P8 LOW-FRE-QUENCY
START ADDRESS OF P11 LOW-FRE-QUENCY
START ADDRESS OF P14 LOW-FRE-QUENCY
START ADDRESS OF OTHERS
START ADDRESS OF FORE & AFT GOP

FIG. 61

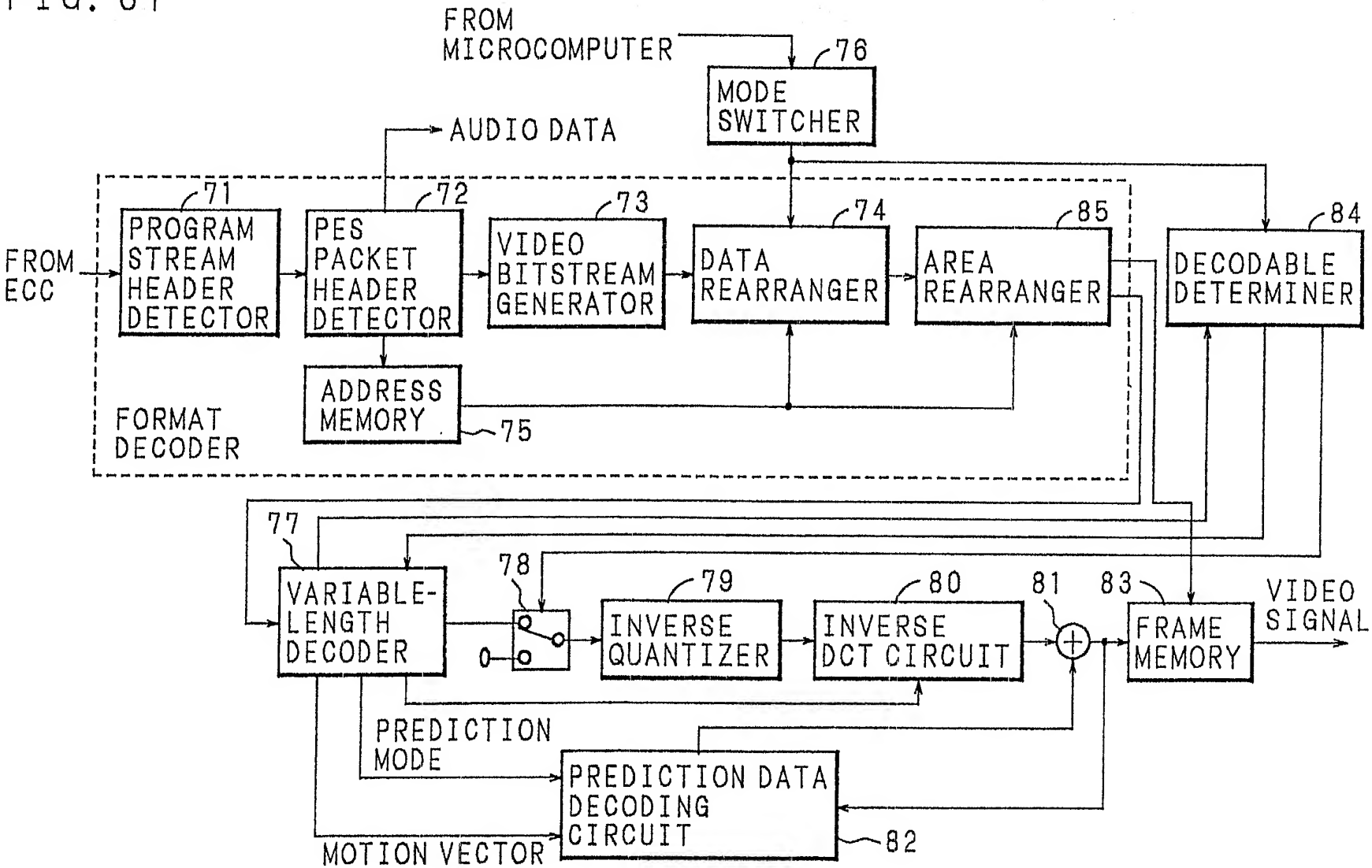

FROM MICROCOMPUTER
76
MODE SWITCHER
AUDIO DATA
71
72
73
74
85
84
FROM ECC
PROGRAM STREAM HEADER DETECTOR
PES PACKET HEADER DETECTOR
VIDEO BITSTREAM GENERATOR
DATA REARRANGER
AREA REARRANGER
DECODABLE DETERMINER
ADDRESS MEMORY
75
FORMAT DECODER
77
78
79
80
81
83
VARIABLE-LENGTH DECODER
INVERSE QUANTIZER
INVERSE DCT CIRCUIT
FRAME MEMORY
VIDEO SIGNAL
PREDICTION MODE
PREDICTION DATA DECODING CIRCUIT
82
MOTION VECTOR

FIG. 62

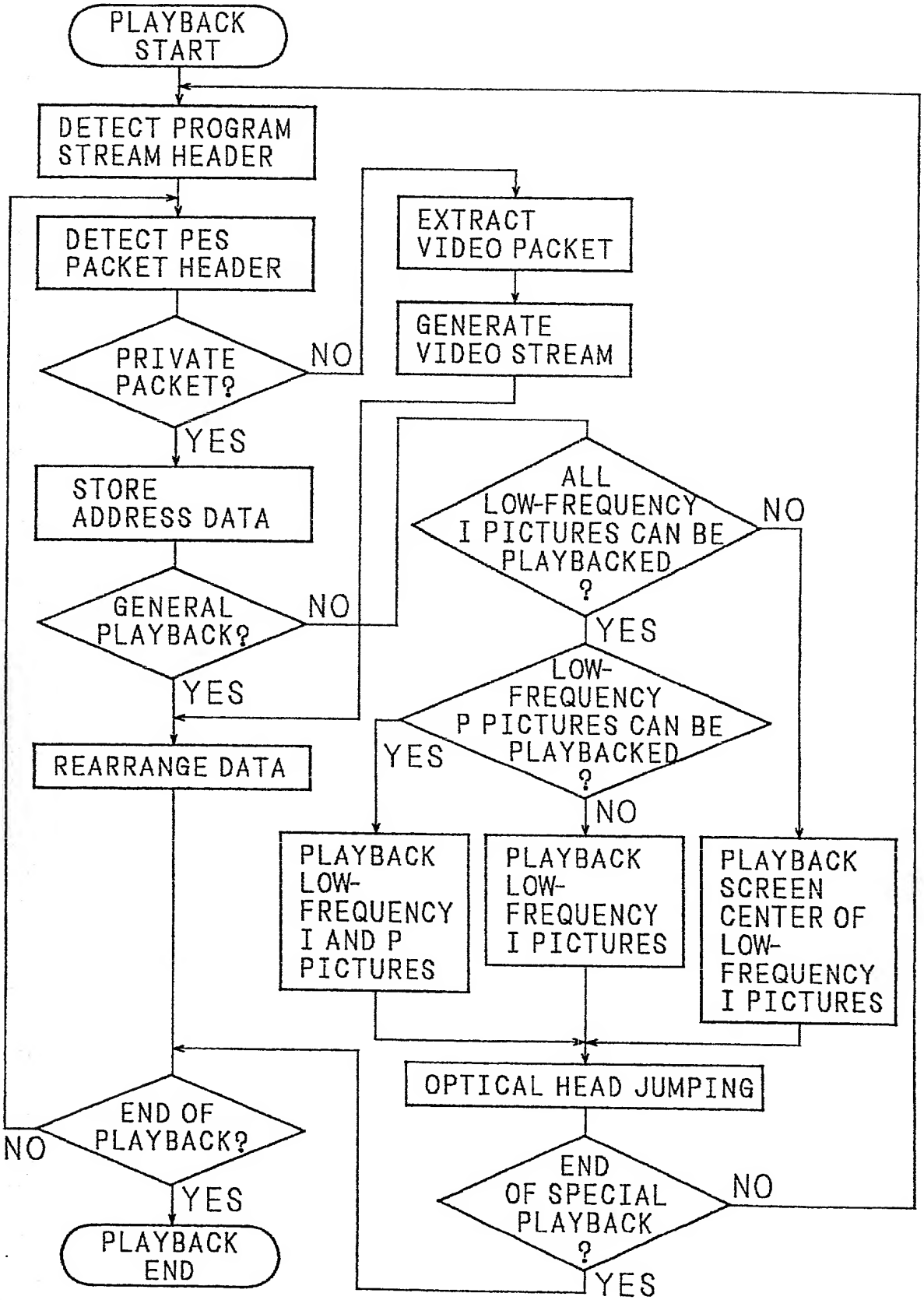

PLAYBACK START
DETECT PROGRAM STREAM HEADER
DETECT PES PACKET HEADER
PRIVATE PACKET?
NO
YES
STORE ADDRESS DATA
GENERAL PLAYBACK?
NO
YES
REARRANGE DATA
EXTRACT VIDEO PACKET
GENERATE VIDEO STREAM
ALL LOW-FREQUENCY I PICTURES CAN BE PLAYBACKED ?
NO
YES
LOW-FREQUENCY P PICTURES CAN BE PLAYBACKED ?
YES
NO
PLAYBACK LOW-FREQUENCY I AND P PICTURES
PLAYBACK LOW-FREQUENCY I PICTURES
PLAYBACK SCREEN CENTER OF LOW-FREQUENCY I PICTURES
OPTICAL HEAD JUMPING
END OF PLAYBACK?
NO
YES
PLAYBACK END
END OF SPECIAL PLAYBACK ?
NO
YES

FIG. 63

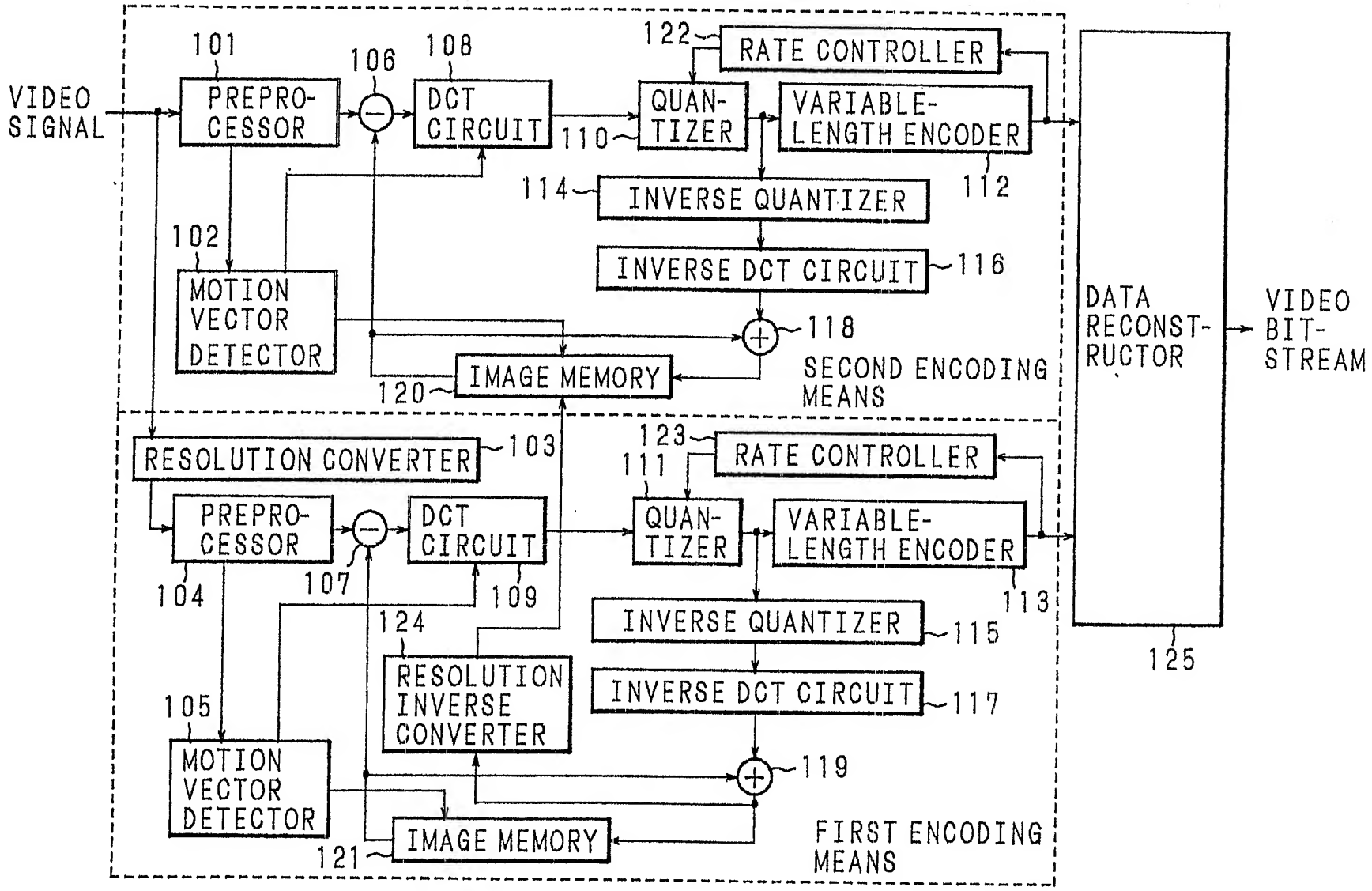

VIDEO SIGNAL
101
PREPRO-CESSOR
106
108
DCT CIRCUIT
110
QUAN-TIZER
122
RATE CONTROLLER
VARIABLE-LENGTH ENCODER
112
114
INVERSE QUANTIZER
102
MOTION VECTOR DETECTOR
INVERSE DCT CIRCUIT
116
118
120
IMAGE MEMORY
SECOND ENCODING MEANS
DATA RECONST-RUCTOR
VIDEO BIT-STREAM
RESOLUTION CONVERTER
103
123
RATE CONTROLLER
111
PREPRO-CESSOR
104
107
DCT CIRCUIT
109
QUAN-TIZER
VARIABLE-LENGTH ENCODER
113
INVERSE QUANTIZER
115
124
RESOLUTION INVERSE CONVERTER
INVERSE DCT CIRCUIT
117
105
MOTION VECTOR DETECTOR
119
121
IMAGE MEMORY
FIRST ENCODING MEANS
125

FIG. 64

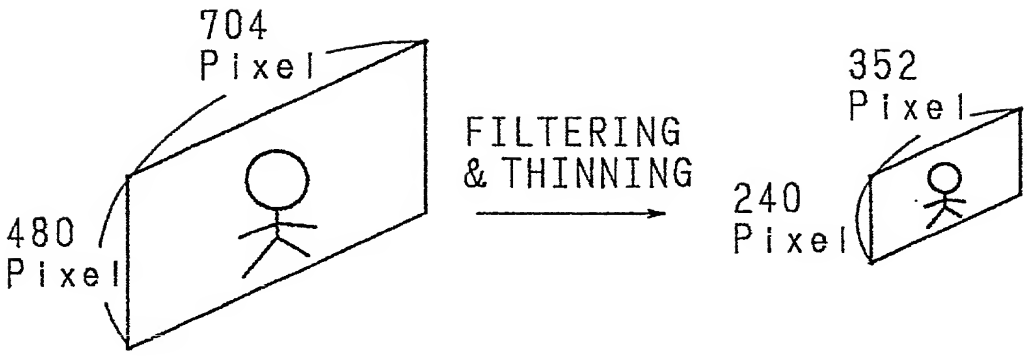


FIG. 65

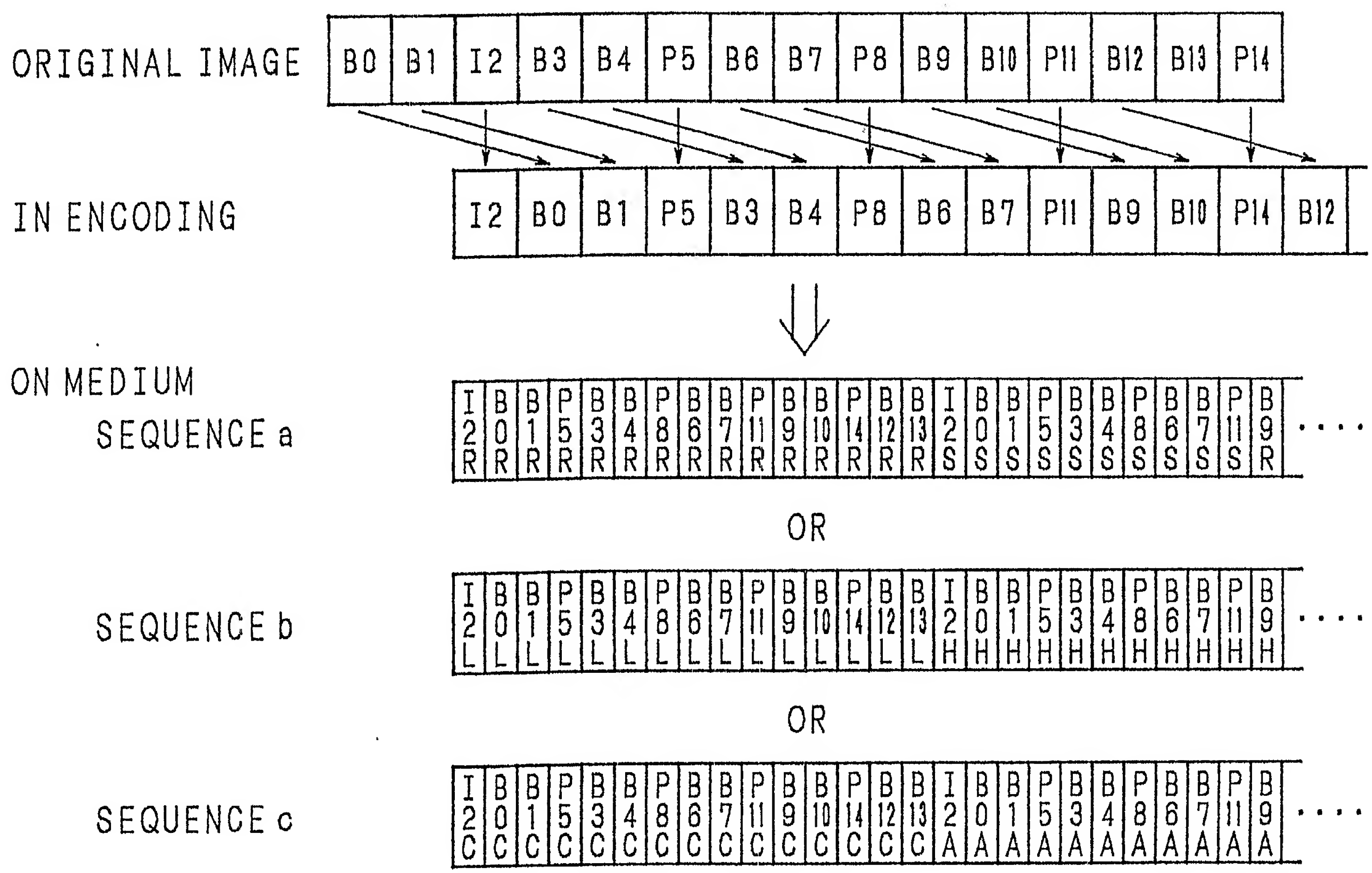

ORIGINAL IMAGE
B0 B1 I2 B3 B4 P5 B6 B7 P8 B9 B10 P11 B12 B13 P14
IN ENCODING
I2 B0 B1 P5 B3 B4 P8 B6 B7 P11 B9 B10 P14 B12
ON MEDIUM
SEQUENCE a
I2R B0R B1R P5R B3R B4R P8R B6R B7R P11R B9R B10R P14R B12R B13R I2S B0S B1S P5S B3S B4S P8S B6S B7S P11S B9R ....
OR
SEQUENCE b
I2L B0L B1L P5L B3L B4L P8L B6L B7L P11L B9L B10L P14L B12L B13L I2H B0H B1H P5H B3H B4H P8H B6H B7H P11H B9H ....
OR
SEQUENCE c
I2C B0C B1C P5C B3C B4C P8C B6C B7C P11C B9C B10C P14C B12C B13C I2A B0A B1A P5A B3A B4A P8A B6A B7A P11A B9A ....

FIG. 66

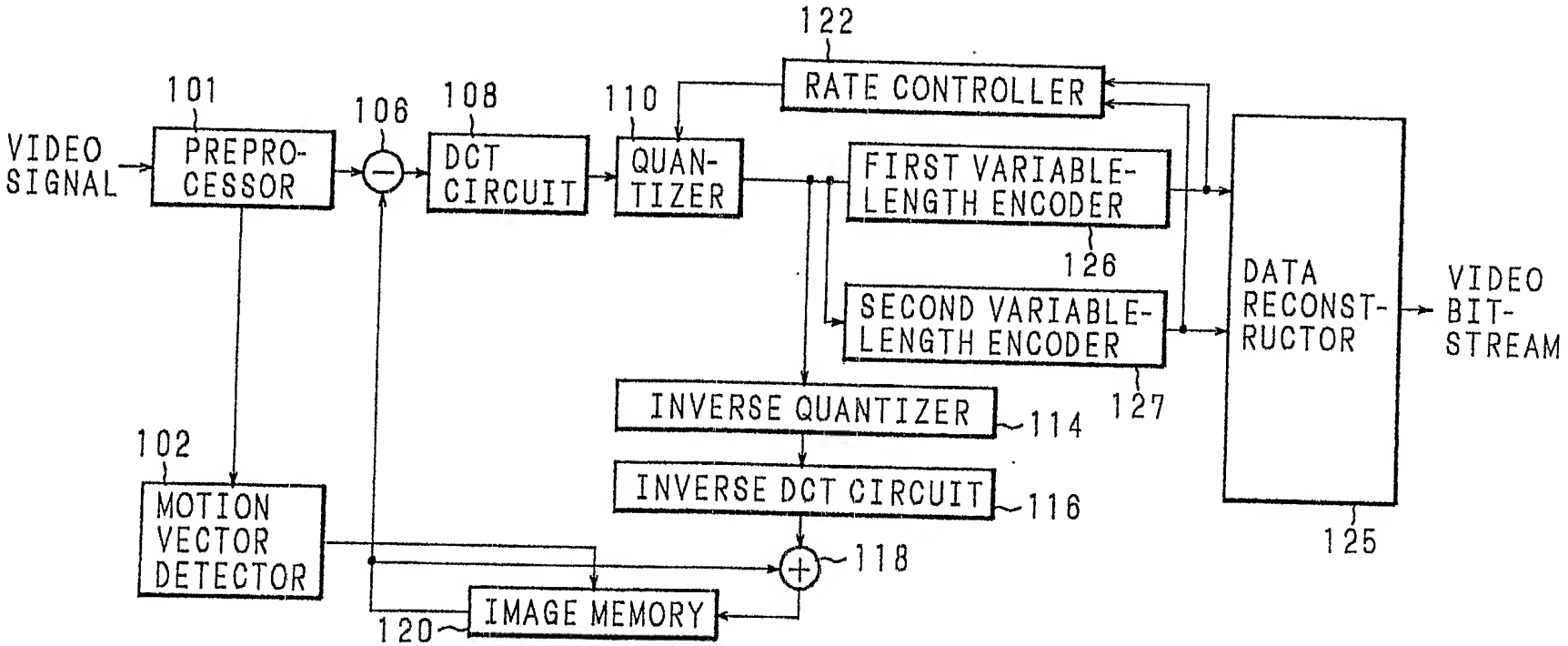

122
RATE CONTROLLER
101
106
108
110
VIDEO SIGNAL
PREPRO-CESSOR
DCT CIRCUIT
QUAN-TIZER
FIRST VARIABLE-LENGTH ENCODER
126
SECOND VARIABLE-LENGTH ENCODER
127
DATA RECONST-RUCTOR
VIDEO BIT-STREAM
INVERSE QUANTIZER
114
INVERSE DCT CIRCUIT
116
118
102
MOTION VECTOR DETECTOR
120
IMAGE MEMORY
125

FIG. 67

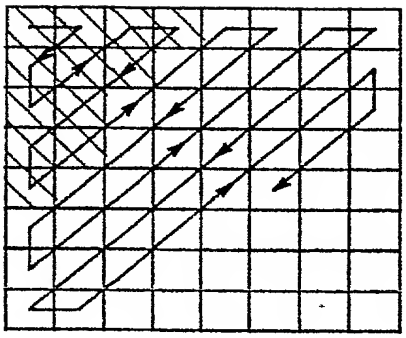


FIG. 68

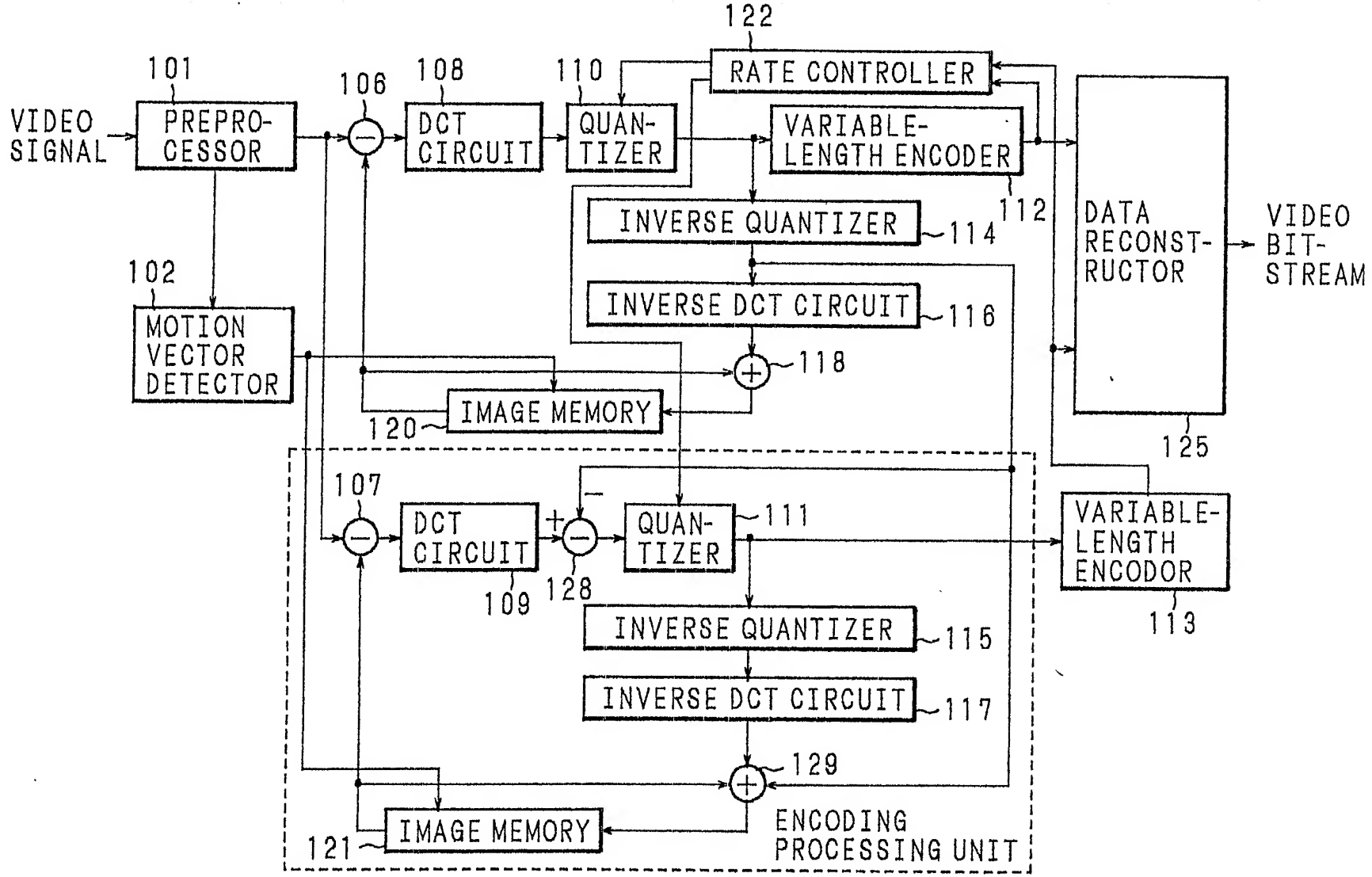

122
RATE CONTROLLER
101
VIDEO SIGNAL
PREPRO-CESSOR
106
108
DCT CIRCUIT
110
QUAN-TIZER
VARIABLE-LENGTH ENCODER
112
INVERSE QUANTIZER
114
INVERSE DCT CIRCUIT
116
118
102
MOTION VECTOR DETECTOR
IMAGE MEMORY
120
DATA RECONST-RUCTOR
VIDEO BIT-STREAM
125
107
DCT CIRCUIT
109
128
QUAN-TIZER
111
VARIABLE-LENGTH ENCODOR
113
INVERSE QUANTIZER
115
INVERSE DCT CIRCUIT
117
129
IMAGE MEMORY
121
ENCODING PROCESSING UNIT

FIG. 69

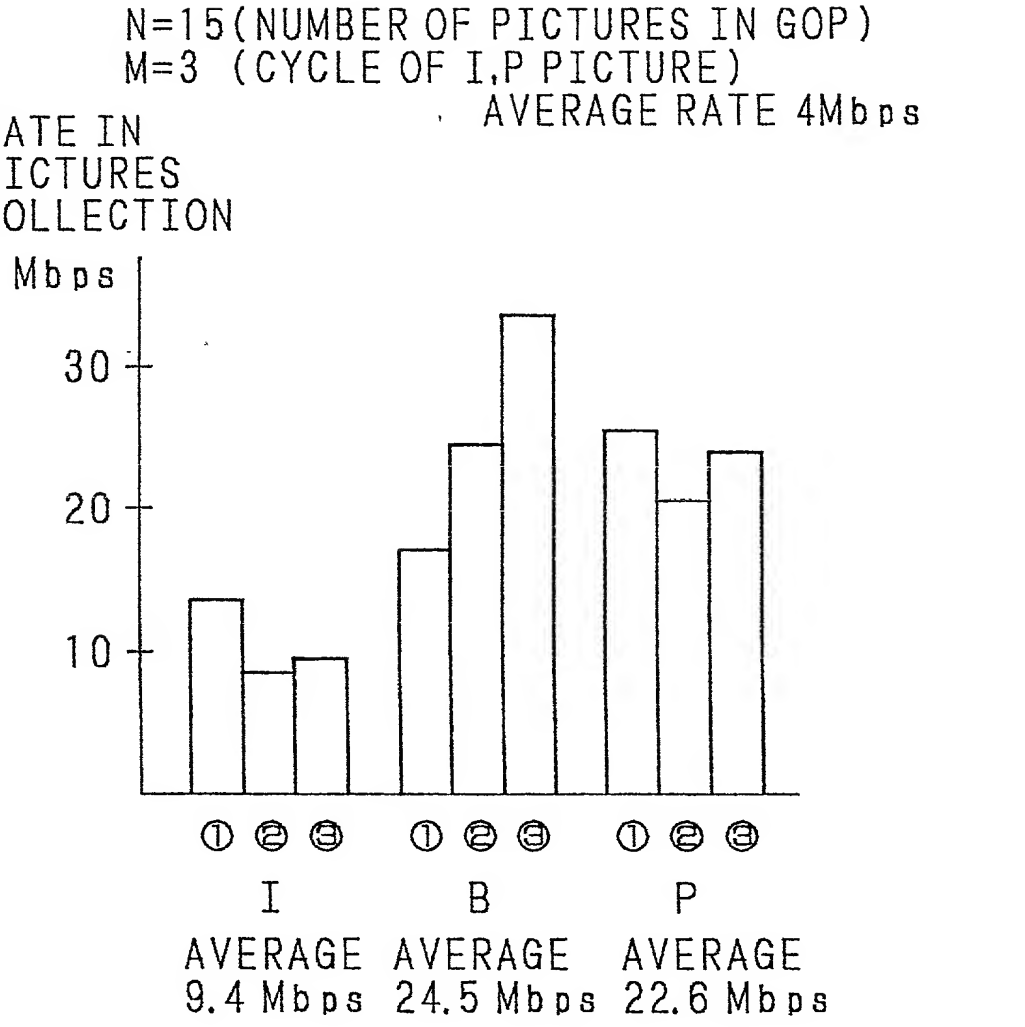

N=15(NUMBER OF PICTURES IN GOP)
M=3 (CYCLE OF I,P PICTURE)
AVERAGE RATE 4Mbps
RATE IN PICTURES COLLECTION
Mbps
30
20
10
① ② ③ ① ② ③ ① ② ③
I
B
P
AVERAGE 9.4 Mbps
AVERAGE 24.5 Mbps
AVERAGE 22.6 Mbps
①:SCENE①
②:SCENE②
③:SCENE③

FIG. 70

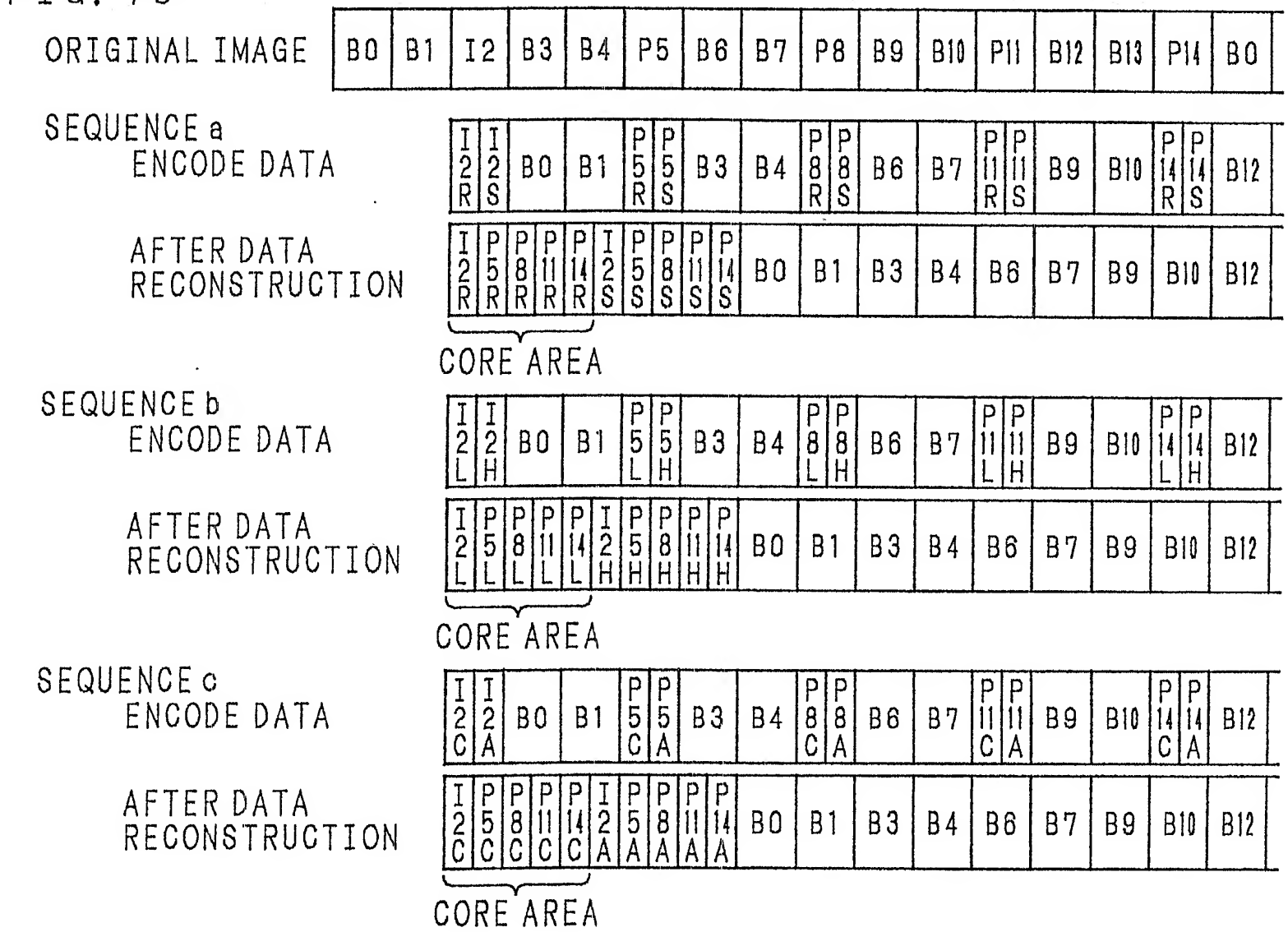

ORIGINAL IMAGE
B0 B1 I2 B3 B4 P5 B6 B7 P8 B9 B10 P11 B12 B13 P14 B0
SEQUENCE a
ENCODE DATA
I2R I2S B0 B1 P5R P5S B3 B4 P8R P8S B6 B7 P11R P11S B9 B10 P14R P14S B12
AFTER DATA RECONSTRUCTION
I2R P5R P8R P11R P14R I2S P5S P8S P11S P14S B0 B1 B3 B4 B6 B7 B9 B10 B12
CORE AREA
SEQUENCE b
ENCODE DATA
I2L I2H B0 B1 P5L P5H B3 B4 P8L P8H B6 B7 P11L P11H B9 B10 P14L P14H B12
AFTER DATA RECONSTRUCTION
I2L P5L P8L P11L P14L I2H P5H P8H P11H P14H B0 B1 B3 B4 B6 B7 B9 B10 B12
CORE AREA
SEQUENCE c
ENCODE DATA
I2C I2A B0 B1 P5C P5A B3 B4 P8C P8A B6 B7 P11C P11A B9 B10 P14C P14A B12
AFTER DATA RECONSTRUCTION
I2C P5C P8C P11C P14C I2A P5A P8A P11A P14A B0 B1 B3 B4 B6 B7 B9 B10 B12
CORE AREA

FIG. 71A

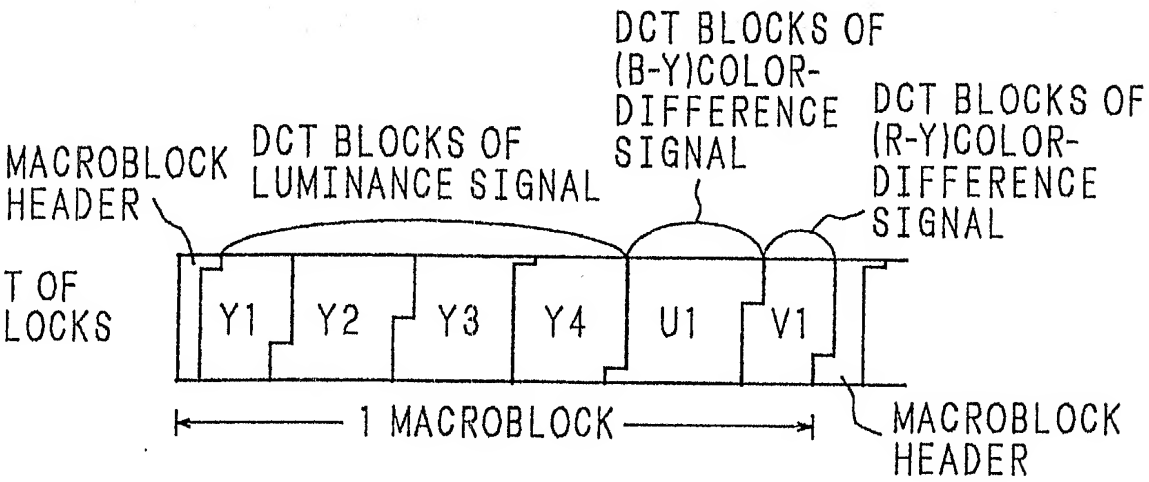


FIG. 71B

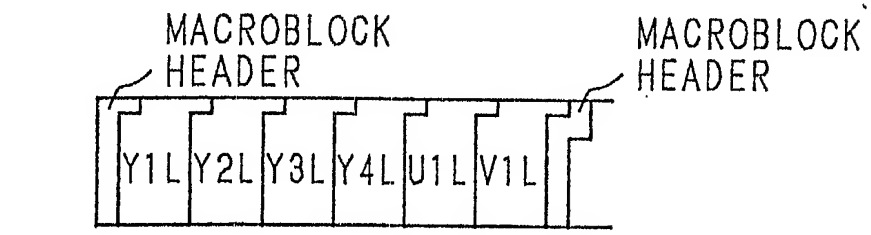


FIG. 71C

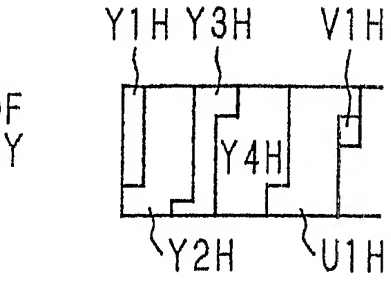


FIG. 71D

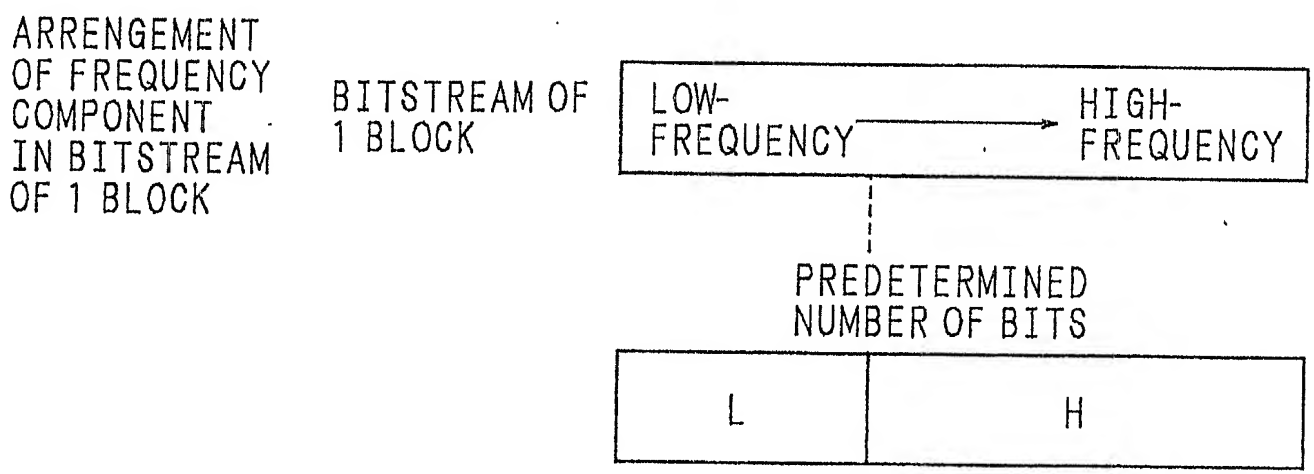

ARRENGEMENT OF FREQUENCY COMPONENT IN BITSTREAM OF 1 BLOCK
BITSTREAM OF 1 BLOCK
LOW-FREQUENCY
HIGH-FREQUENCY
PREDETERMINED NUMBER OF BITS
L
H

FIG. 72A

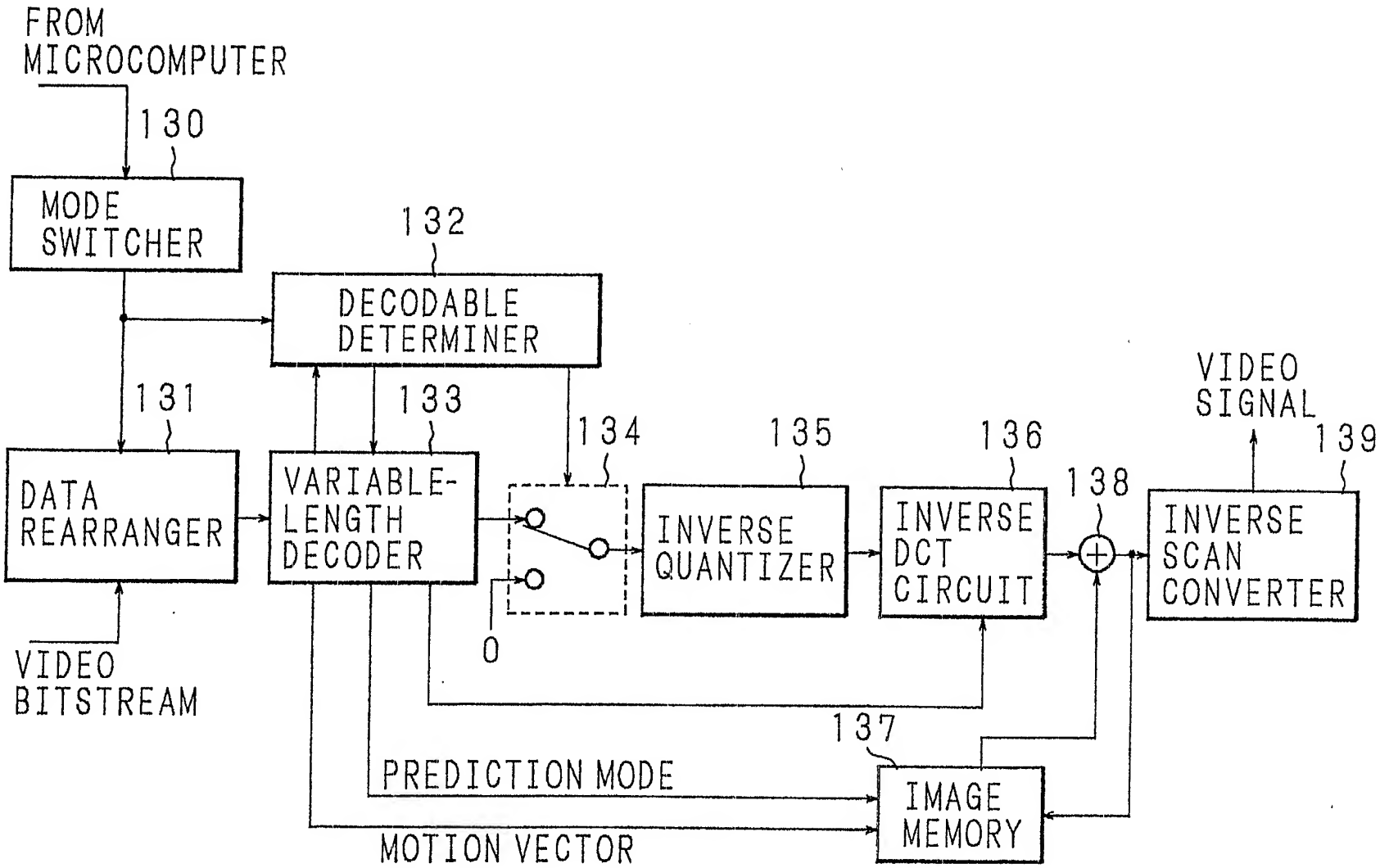

FROM MICROCOMPUTER
130
MODE SWITCHER
132
DECODABLE DETERMINER
131
133
134
135
136
138
VIDEO SIGNAL
139
DATA REARRANGER
VARIABLE-LENGTH DECODER
INVERSE QUANTIZER
INVERSE DCT CIRCUIT
INVERSE SCAN CONVERTER
0
VIDEO BITSTREAM
137
PREDICTION MODE
IMAGE MEMORY
MOTION VECTOR

FIG. 72B

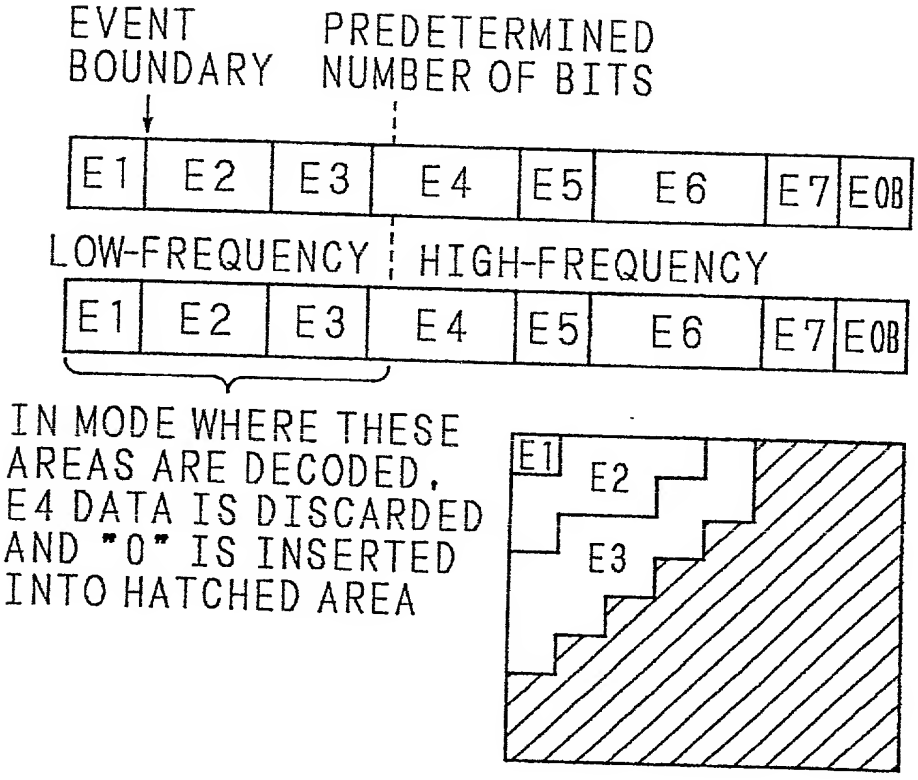

EVENT BOUNDARY
PREDETERMINED NUMBER OF BITS
E1
E2
E3
E4
E5
E6
E7
EOB
LOW-FREQUENCY
HIGH-FREQUENCY
E1
E2
E3
E4
E5
E6
E7
EOB
IN MODE WHERE THESE AREAS ARE DECODED, E4 DATA IS DISCARDED AND "0" IS INSERTED INTO HATCHED AREA
E1
E2
E3

FIG. 73A

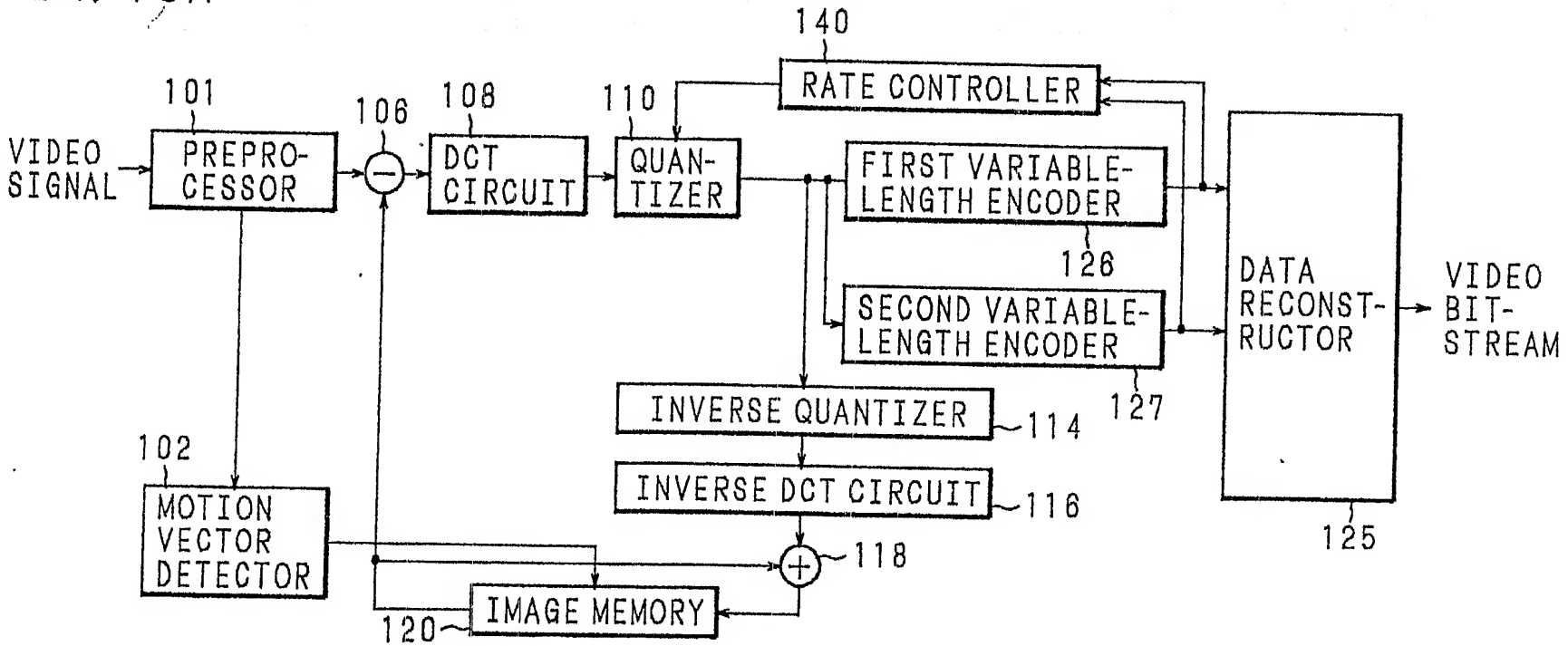


FIG. 73B

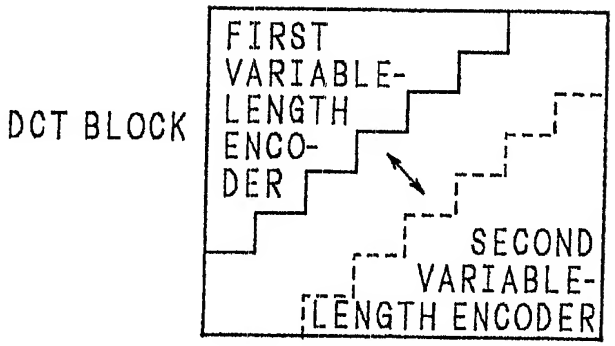


FIG. 74

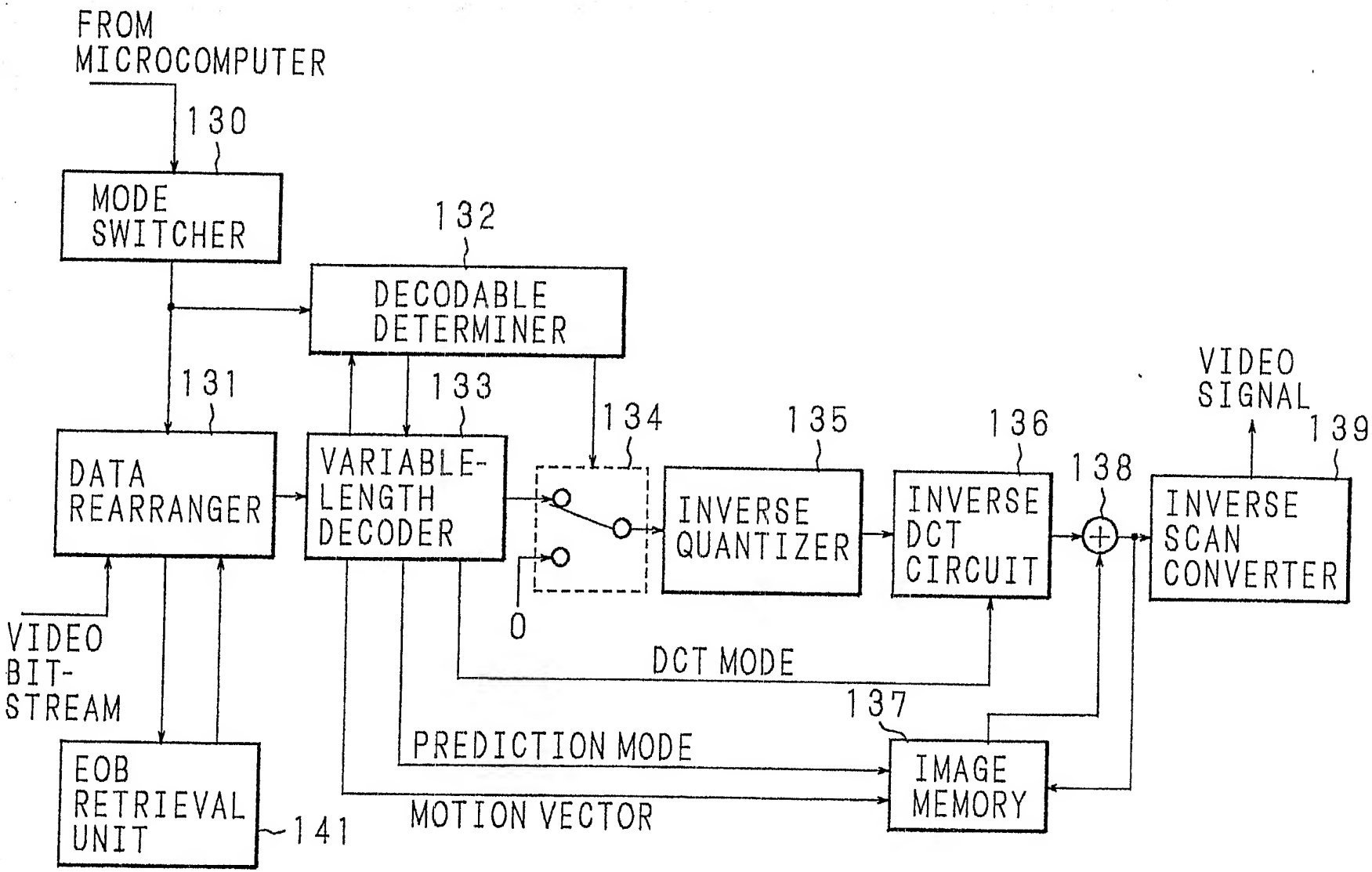

FROM MICROCOMPUTER
130
MODE SWITCHER
132
DECODABLE DETERMINER
131
133
134
135
136
138
VIDEO SIGNAL
139
DATA REARRANGER
VARIABLE-LENGTH DECODER
INVERSE QUANTIZER
INVERSE DCT CIRCUIT
INVERSE SCAN CONVERTER
0
VIDEO BIT-STREAM
DCT MODE
137
PREDICTION MODE
EOB RETRIEVAL UNIT
141
MOTION VECTOR
IMAGE MEMORY

FIG. 75

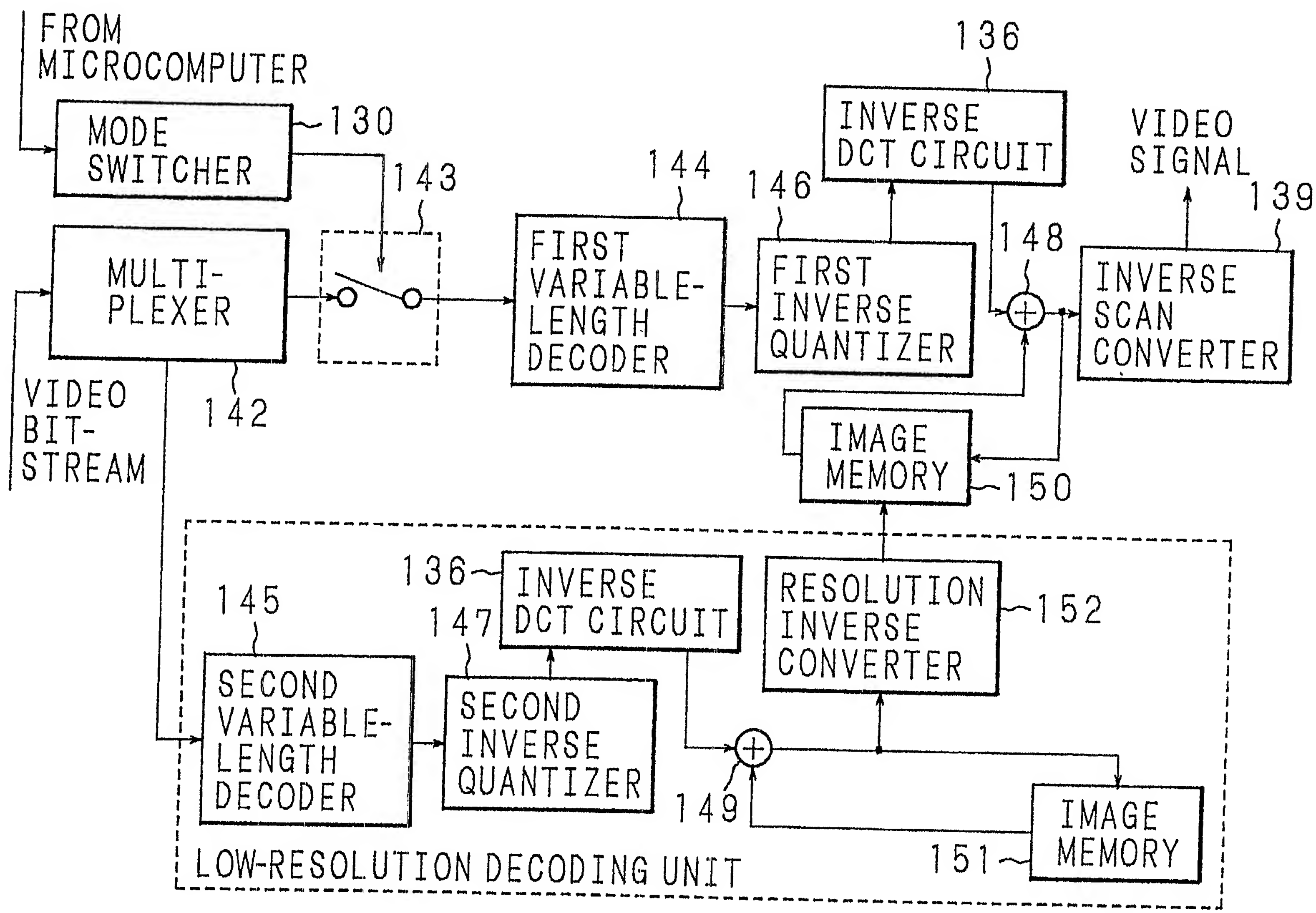

FROM MICROCOMPUTER
MODE SWITCHER
130
MULTI-PLEXER
142
VIDEO BIT-STREAM
143
FIRST VARIABLE-LENGTH DECODER
144
FIRST INVERSE QUANTIZER
146
INVERSE DCT CIRCUIT
136
148
INVERSE SCAN CONVERTER
139
VIDEO SIGNAL
IMAGE MEMORY
150
SECOND VARIABLE-LENGTH DECODER
145
SECOND INVERSE QUANTIZER
147
INVERSE DCT CIRCUIT
136
149
RESOLUTION INVERSE CONVERTER
152
IMAGE MEMORY
151
LOW-RESOLUTION DECODING UNIT

FIG. 76

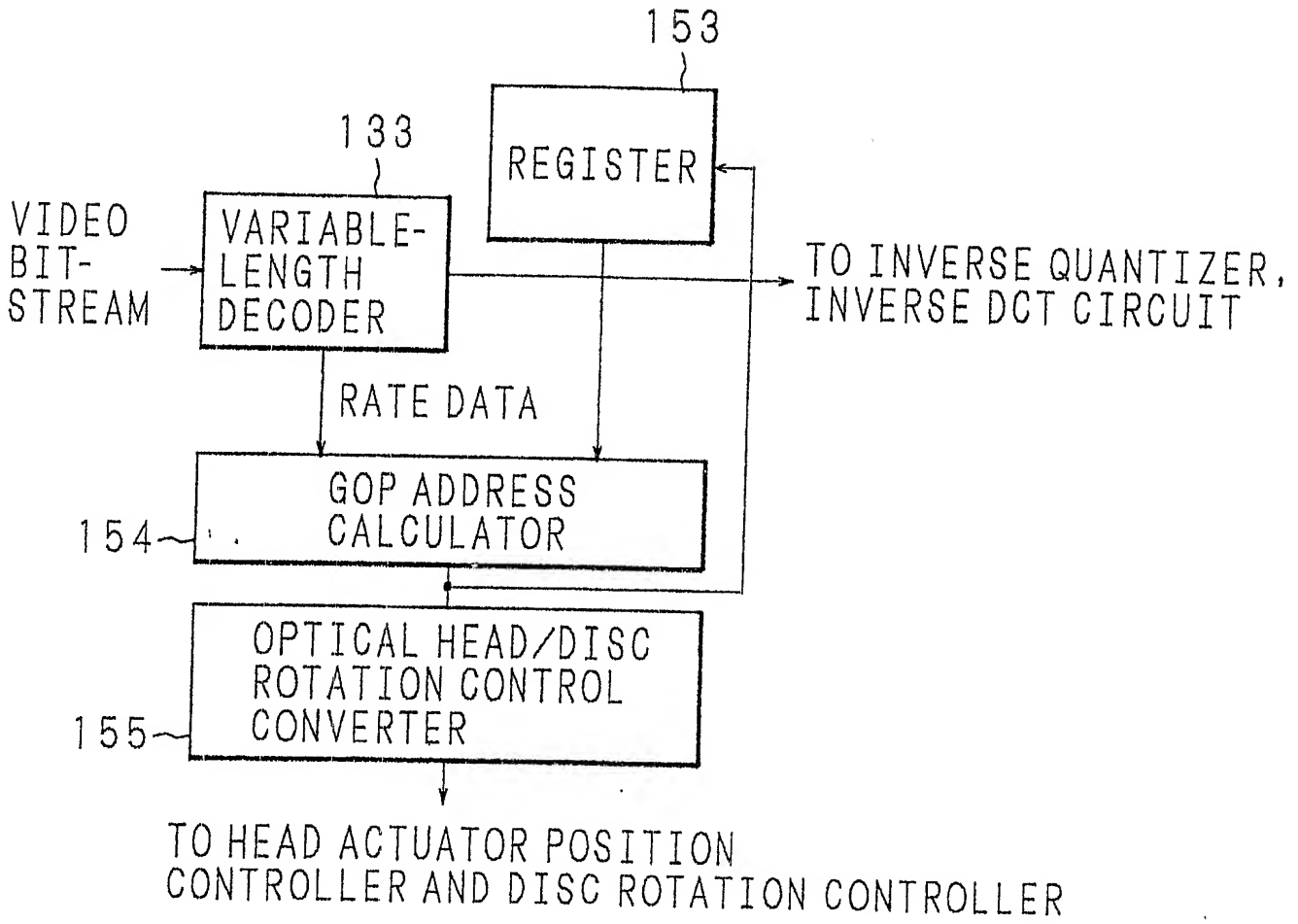
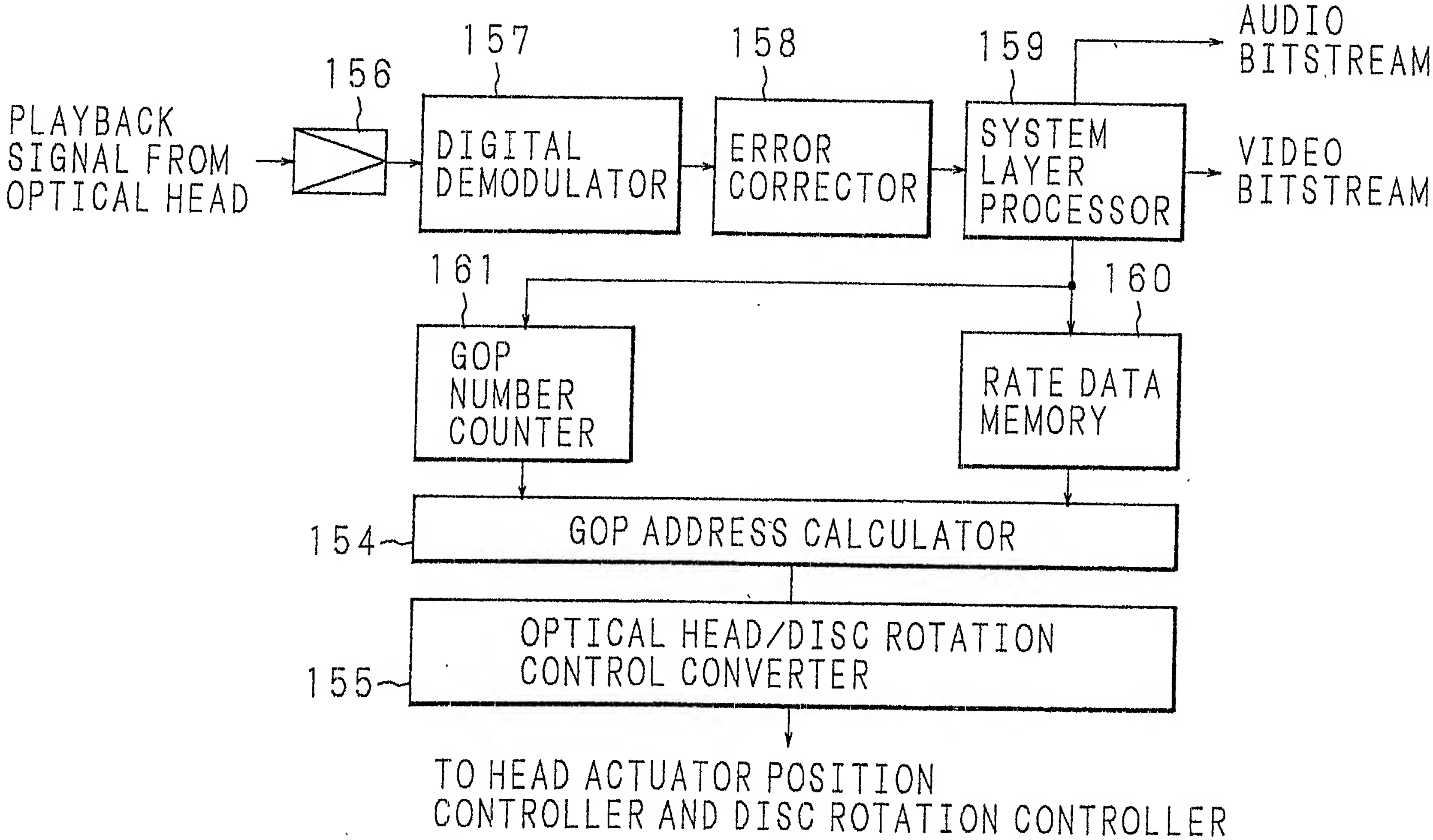

153
REGISTER
133
VIDEO BIT-STREAM
VARIABLE-LENGTH DECODER
TO INVERSE QUANTIZER, INVERSE DCT CIRCUIT
RATE DATA
154
GOP ADDRESS CALCULATOR
155
OPTICAL HEAD/DISC ROTATION CONTROL CONVERTER
TO HEAD ACTUATOR POSITION CONTROLLER AND DISC ROTATION CONTROLLER

FIG. 77



PLAYBACK SIGNAL FROM OPTICAL HEAD
156
157
DIGITAL DEMODULATOR
158
ERROR CORRECTOR
159
SYSTEM LAYER PROCESSOR
AUDIO BITSTREAM
VIDEO BITSTREAM
161
GOP NUMBER COUNTER
160
RATE DATA MEMORY
154
GOP ADDRESS CALCULATOR
155
OPTICAL HEAD/DISC ROTATION CONTROL CONVERTER
TO HEAD ACTUATOR POSITION CONTROLLER AND DISC ROTATION CONTROLLER

FIG. 78

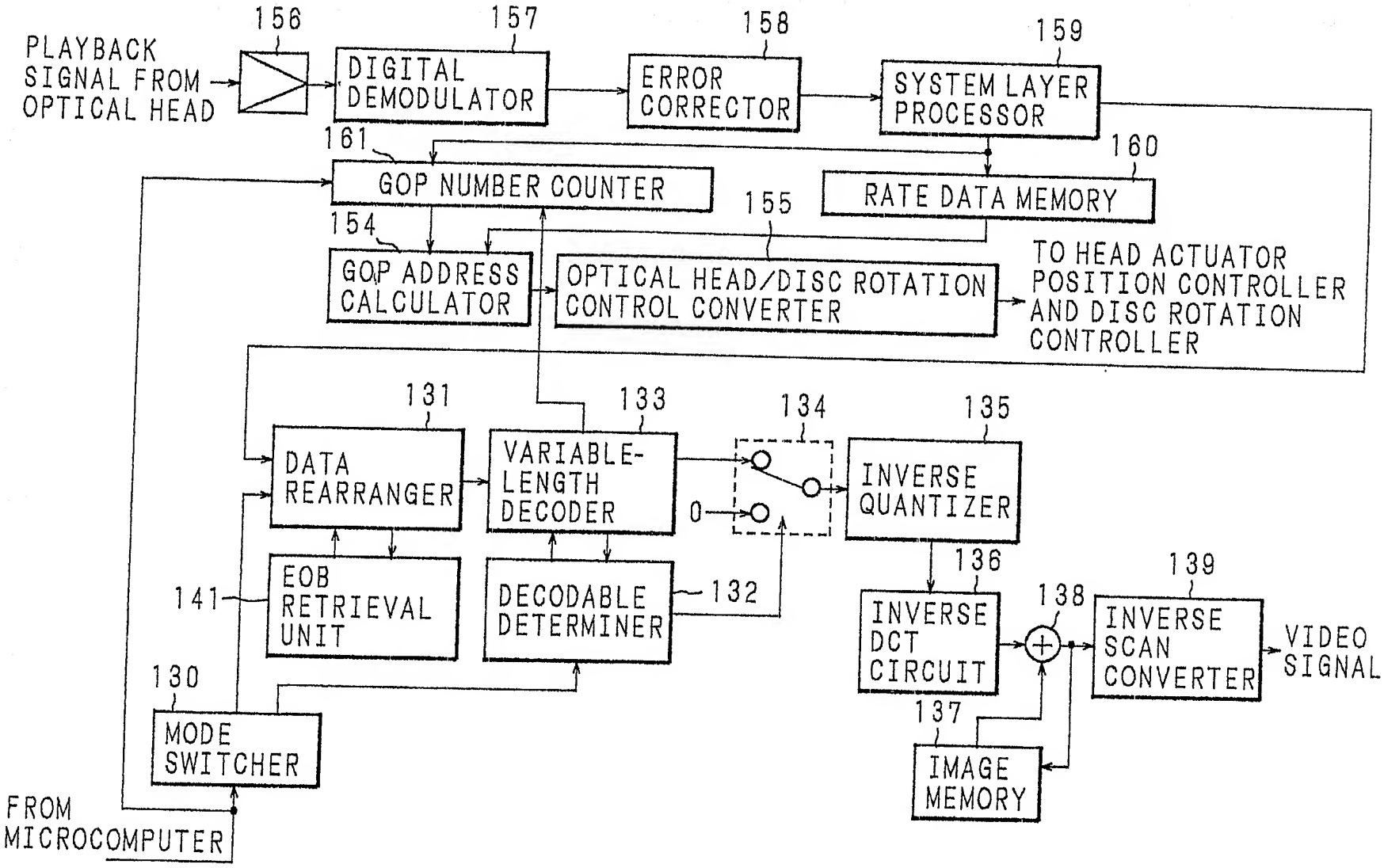

156
157
158
159
PLAYBACK SIGNAL FROM OPTICAL HEAD
DIGITAL DEMODULATOR
ERROR CORRECTOR
SYSTEM LAYER PROCESSOR
161
160
GOP NUMBER COUNTER
RATE DATA MEMORY
155
154
GOP ADDRESS CALCULATOR
OPTICAL HEAD/DISC ROTATION CONTROL CONVERTER
TO HEAD ACTUATOR POSITION CONTROLLER AND DISC ROTATION CONTROLLER
131
133
134
135
DATA REARRANGER
VARIABLE-LENGTH DECODER
0
INVERSE QUANTIZER
136
139
141
EOB RETRIEVAL UNIT
DECODABLE DETERMINER
132
138
INVERSE DCT CIRCUIT
INVERSE SCAN CONVERTER
VIDEO SIGNAL
130
137
MODE SWITCHER
IMAGE MEMORY
FROM MICROCOMPUTER

FIG. 79

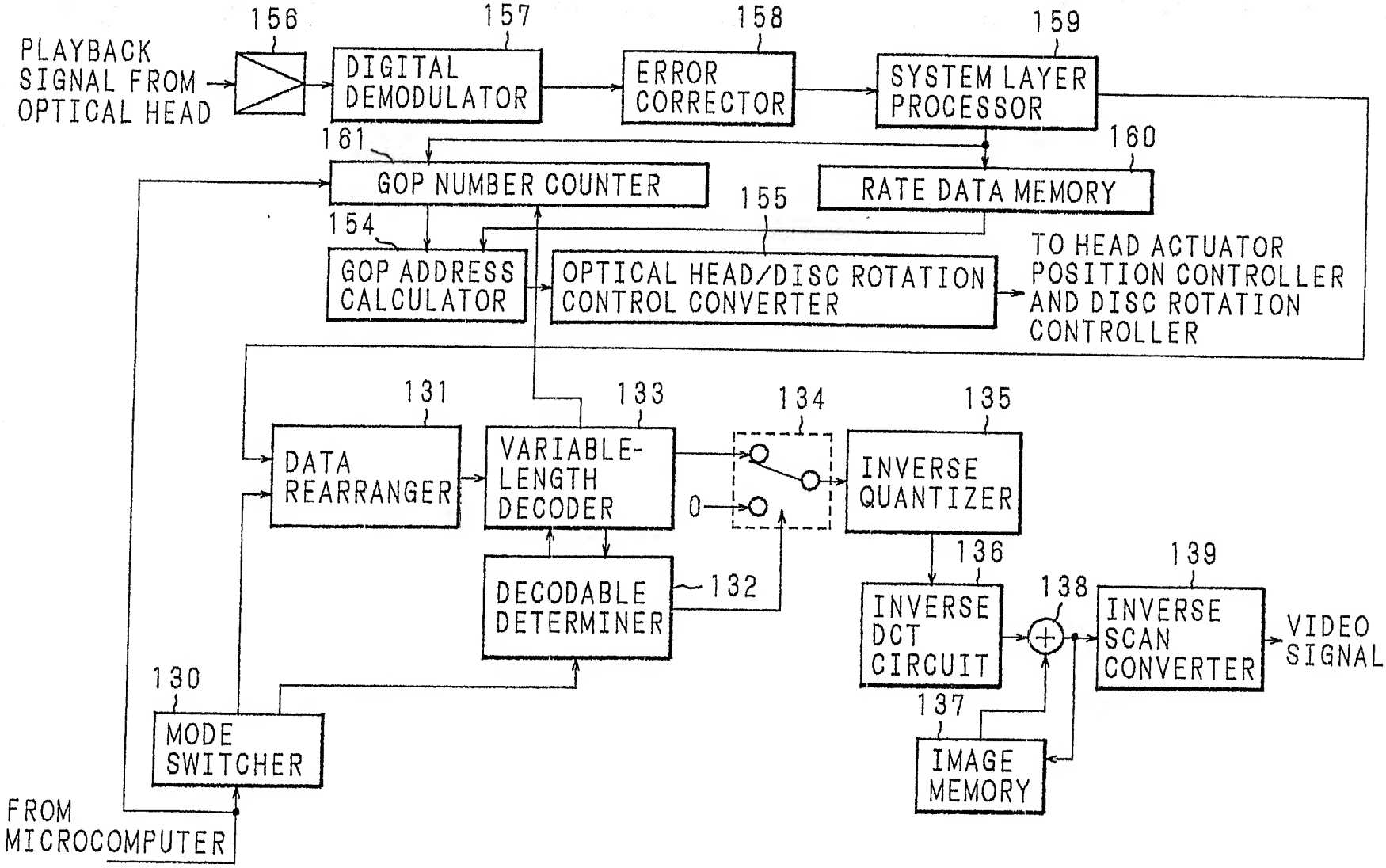

156
157
158
159
PLAYBACK SIGNAL FROM OPTICAL HEAD
DIGITAL DEMODULATOR
ERROR CORRECTOR
SYSTEM LAYER PROCESSOR
161
160
GOP NUMBER COUNTER
RATE DATA MEMORY
155
154
GOP ADDRESS CALCULATOR
OPTICAL HEAD/DISC ROTATION CONTROL CONVERTER
TO HEAD ACTUATOR POSITION CONTROLLER AND DISC ROTATION CONTROLLER
131
133
134
135
DATA REARRANGER
VARIABLE-LENGTH DECODER
0
INVERSE QUANTIZER
136
139
DECODABLE DETERMINER
132
138
INVERSE DCT CIRCUIT
INVERSE SCAN CONVERTER
VIDEO SIGNAL
130
137
MODE SWITCHER
IMAGE MEMORY
FROM MICROCOMPUTER

FIG. 80

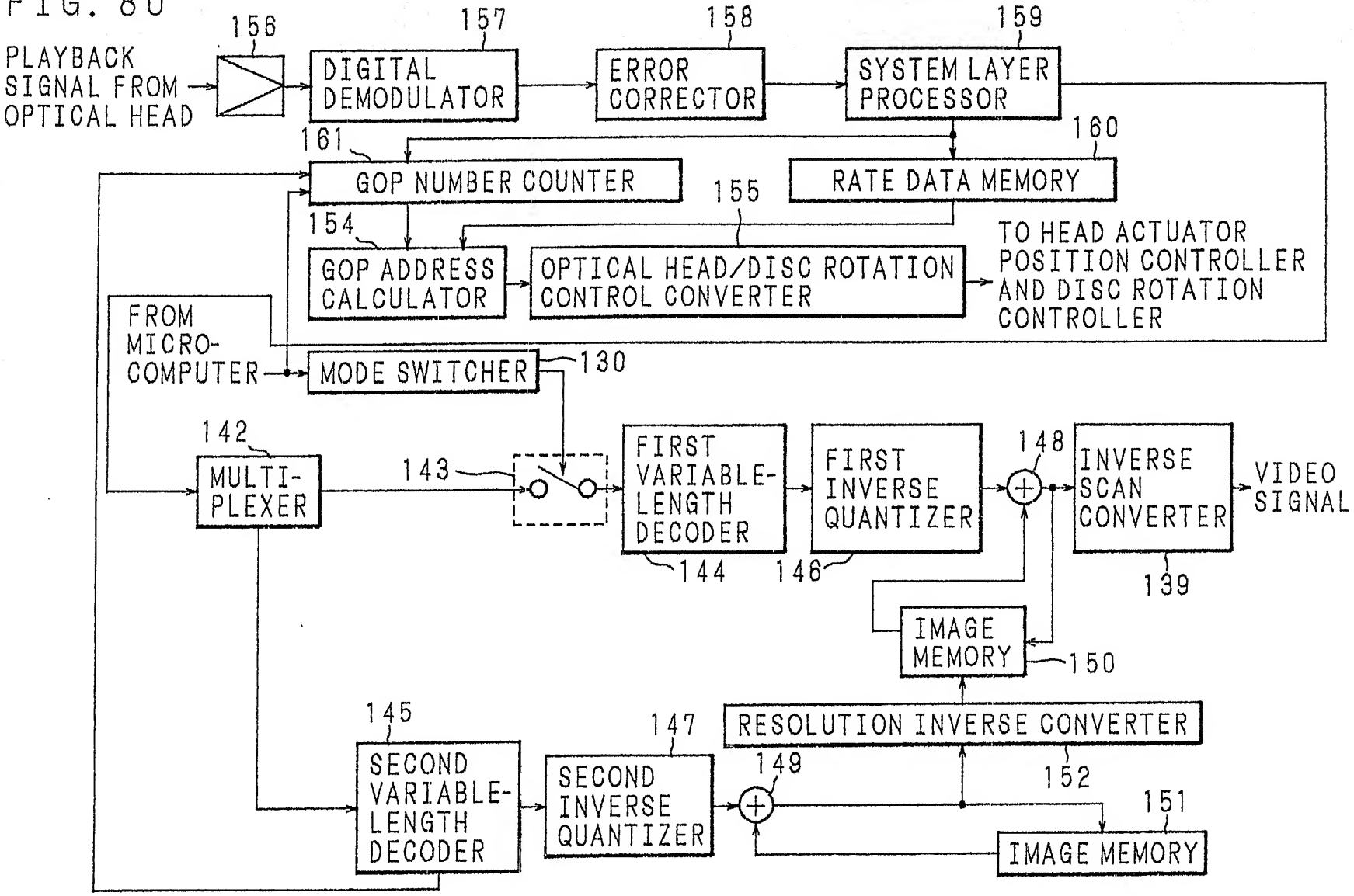

156
157
158
159
PLAYBACK SIGNAL FROM OPTICAL HEAD
DIGITAL DEMODULATOR
ERROR CORRECTOR
SYSTEM LAYER PROCESSOR
161
160
GOP NUMBER COUNTER
RATE DATA MEMORY
155
154
GOP ADDRESS CALCULATOR
OPTICAL HEAD/DISC ROTATION CONTROL CONVERTER
TO HEAD ACTUATOR POSITION CONTROLLER AND DISC ROTATION CONTROLLER
FROM MICRO-COMPUTER
MODE SWITCHER
130
142
143
148
MULTI-PLEXER
FIRST VARIABLE-LENGTH DECODER
FIRST INVERSE QUANTIZER
INVERSE SCAN CONVERTER
VIDEO SIGNAL
144
146
139
IMAGE MEMORY
150
145
147
RESOLUTION INVERSE CONVERTER
149
152
151
SECOND VARIABLE-LENGTH DECODER
SECOND INVERSE QUANTIZER
IMAGE MEMORY

FIG. 81

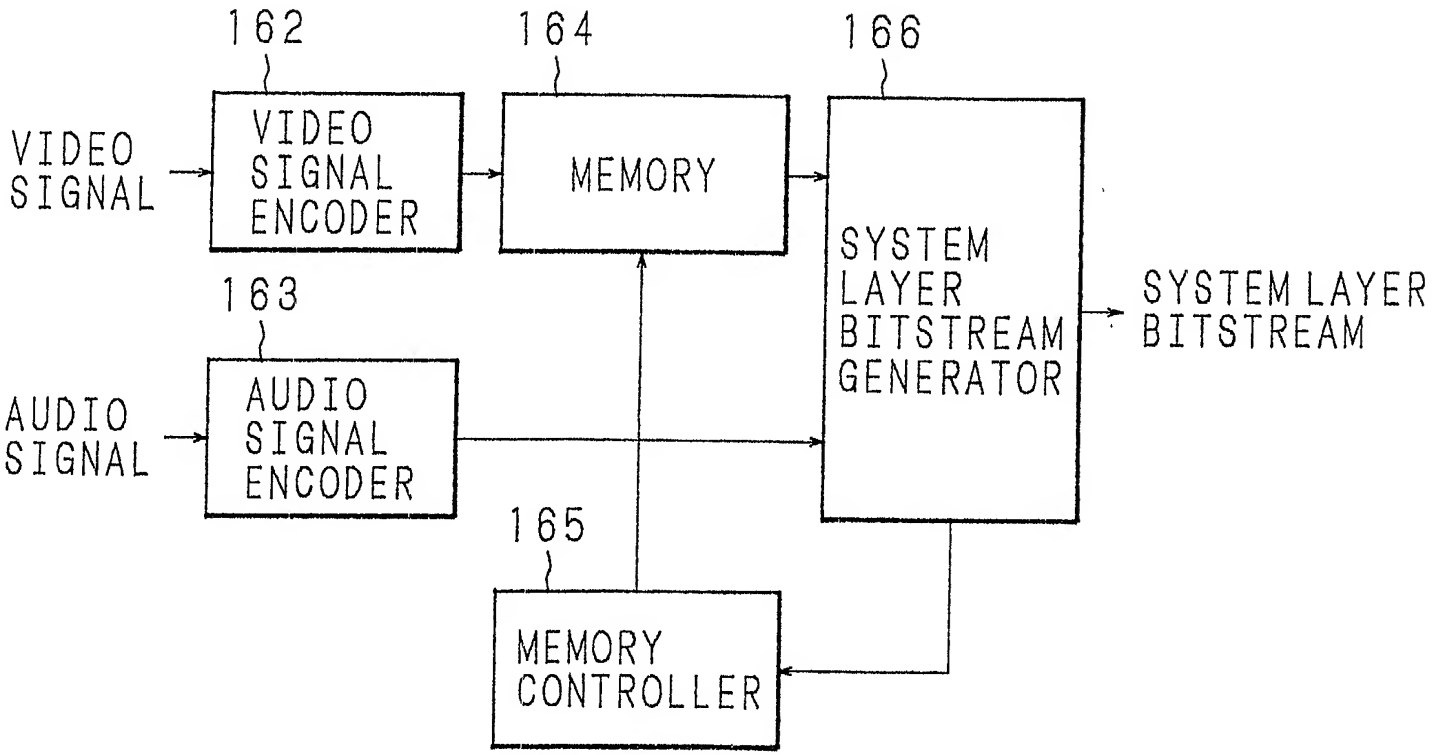
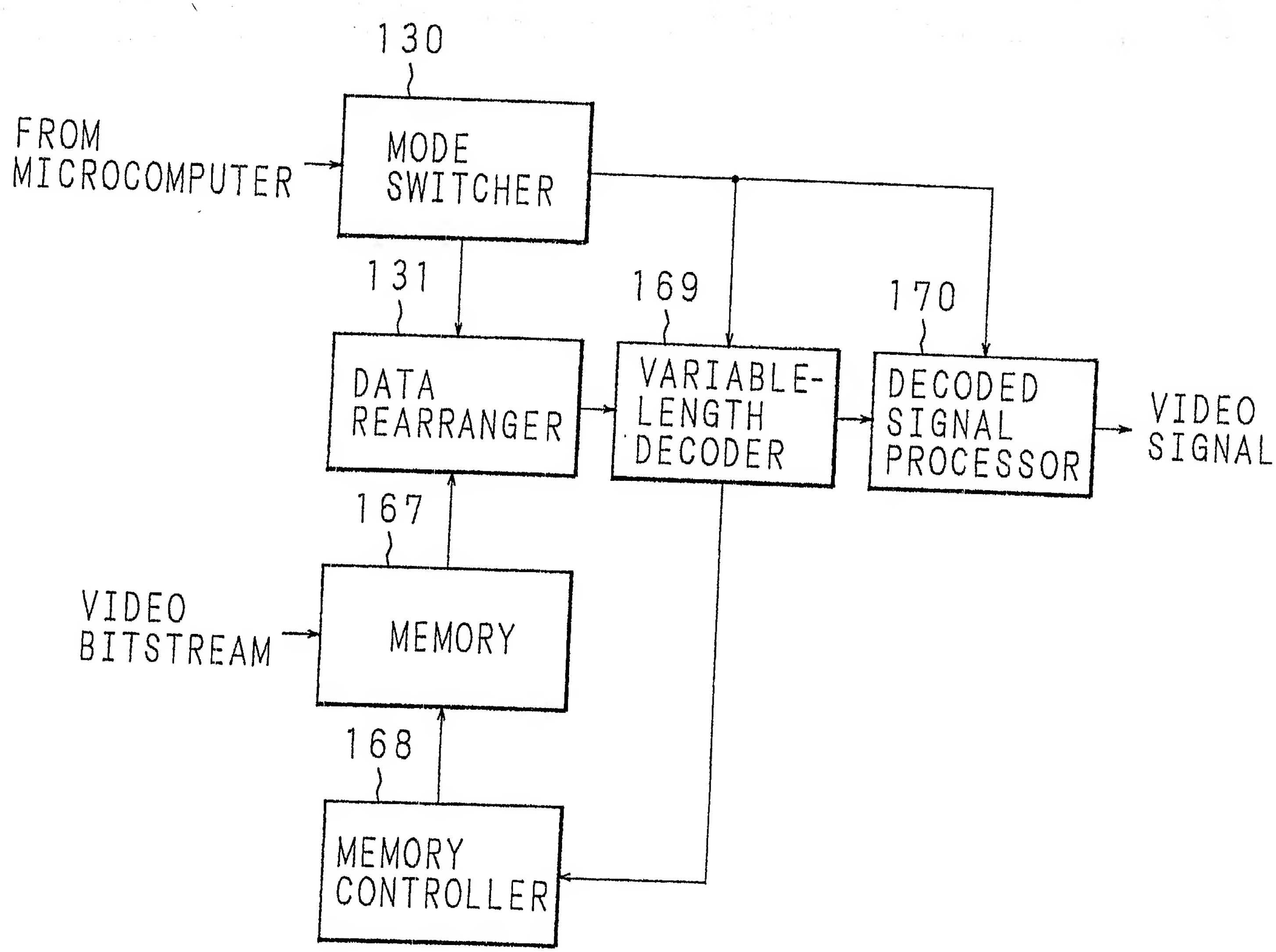

162
164
166
VIDEO SIGNAL
VIDEO SIGNAL ENCODER
MEMORY
SYSTEM LAYER BITSTREAM GENERATOR
SYSTEM LAYER BITSTREAM
163
AUDIO SIGNAL
AUDIO SIGNAL ENCODER
165
MEMORY CONTROLLER

FIG. 82



130
FROM MICROCOMPUTER
MODE SWITCHER
131
DATA REARRANGER
169
VARIABLE-LENGTH DECODER
170
DECODED SIGNAL PROCESSOR
VIDEO SIGNAL
167
VIDEO BITSTREAM
MEMORY
168
MEMORY CONTROLLER

FIG. 83A

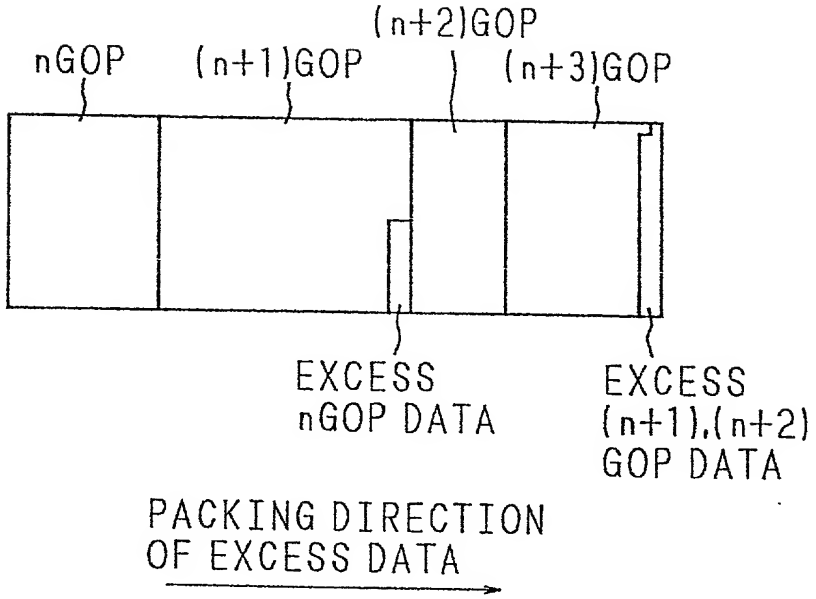


FIG. 83B

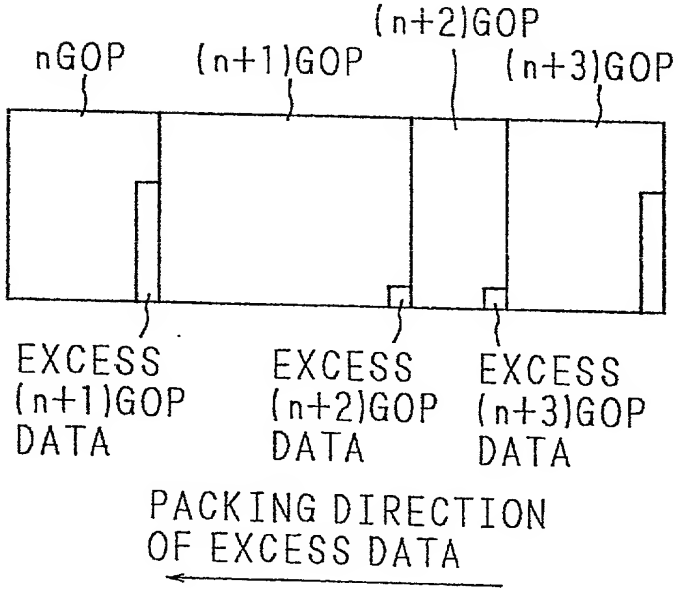


FIG. 84

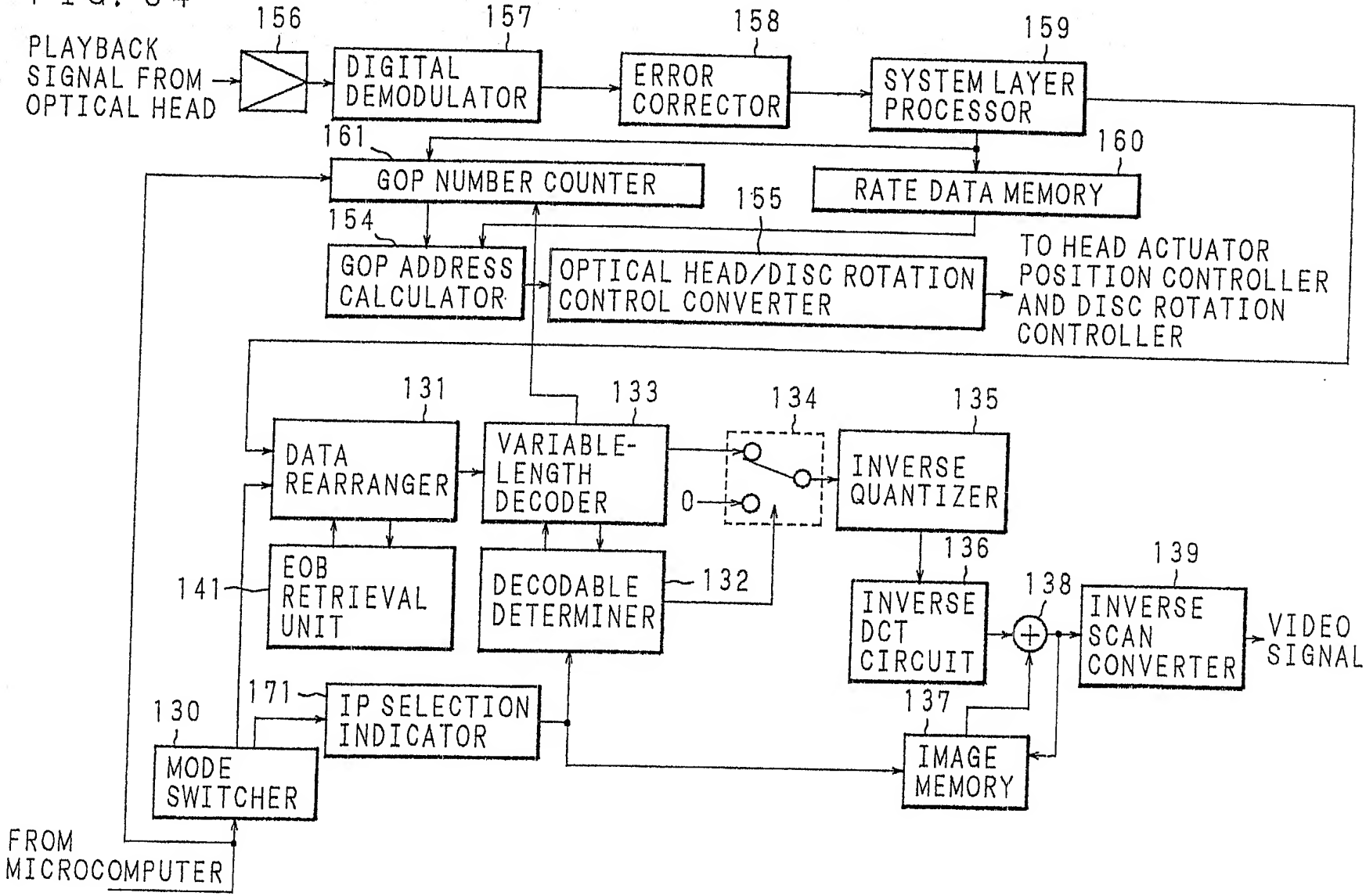

PLAYBACK SIGNAL FROM OPTICAL HEAD
156
157
DIGITAL DEMODULATOR
158
ERROR CORRECTOR
159
SYSTEM LAYER PROCESSOR
161
GOP NUMBER COUNTER
160
RATE DATA MEMORY
155
154
GOP ADDRESS CALCULATOR
OPTICAL HEAD/DISC ROTATION CONTROL CONVERTER
TO HEAD ACTUATOR POSITION CONTROLLER AND DISC ROTATION CONTROLLER
131
133
134
135
DATA REARRANGER
VARIABLE-LENGTH DECODER
0
INVERSE QUANTIZER
136
139
EOB RETRIEVAL UNIT
141
DECODABLE DETERMINER
132
138
INVERSE DCT CIRCUIT
INVERSE SCAN CONVERTER
VIDEO SIGNAL
171
IP SELECTION INDICATOR
130
137
MODE SWITCHER
IMAGE MEMORY
FROM MICROCOMPUTER

FIG. 85

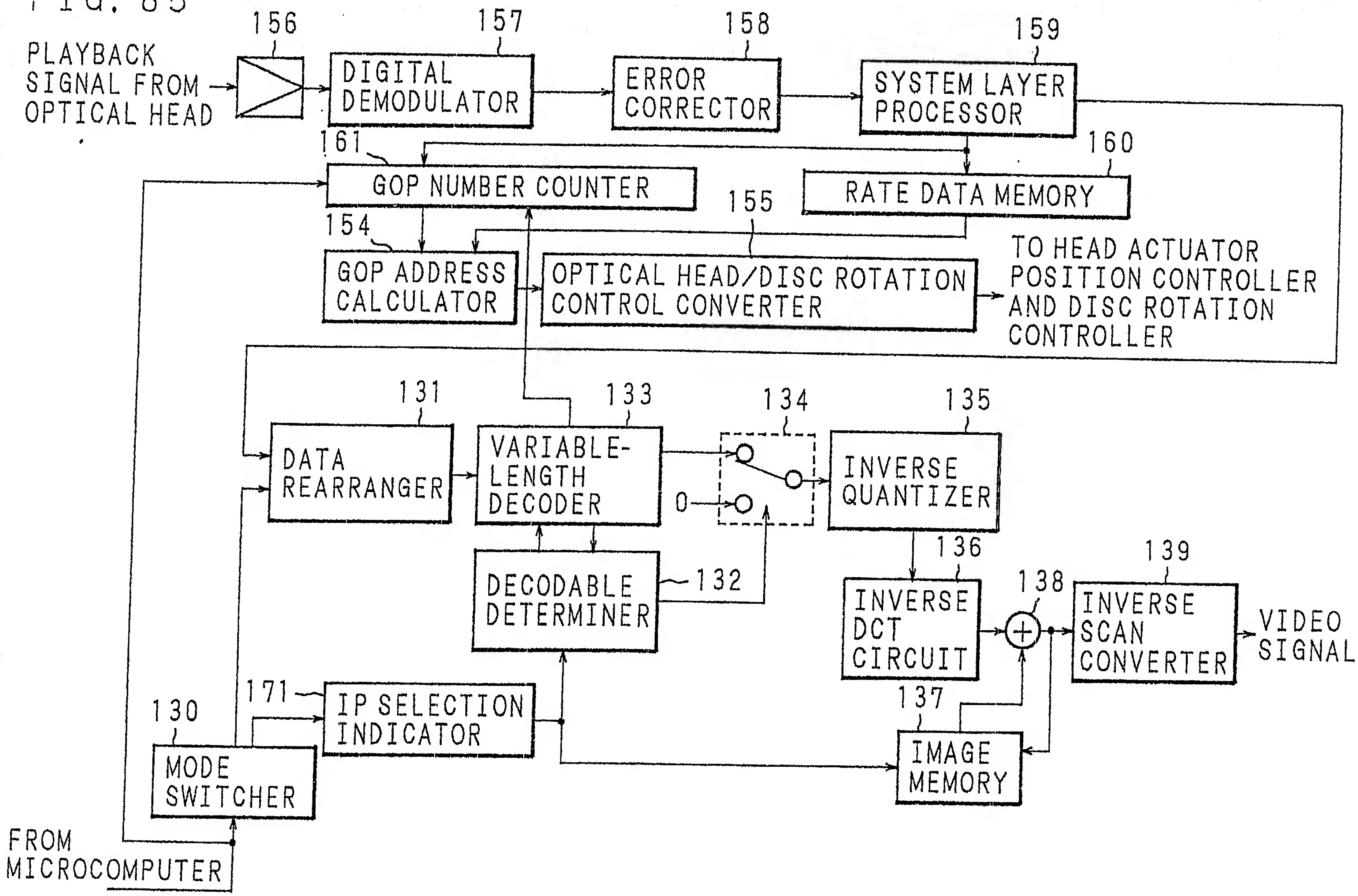

PLAYBACK SIGNAL FROM OPTICAL HEAD
156
157
DIGITAL DEMODULATOR
158
ERROR CORRECTOR
159
SYSTEM LAYER PROCESSOR
161
GOP NUMBER COUNTER
160
RATE DATA MEMORY
154
GOP ADDRESS CALCULATOR
155
OPTICAL HEAD/DISC ROTATION CONTROL CONVERTER
TO HEAD ACTUATOR POSITION CONTROLLER AND DISC ROTATION CONTROLLER
131
DATA REARRANGER
133
VARIABLE-LENGTH DECODER
134
0
135
INVERSE QUANTIZER
132
DECODABLE DETERMINER
136
INVERSE DCT CIRCUIT
138
139
INVERSE SCAN CONVERTER
VIDEO SIGNAL
137
IMAGE MEMORY
171
IP SELECTION INDICATOR
130
MODE SWITCHER
FROM MICROCOMPUTER

FIG. 86

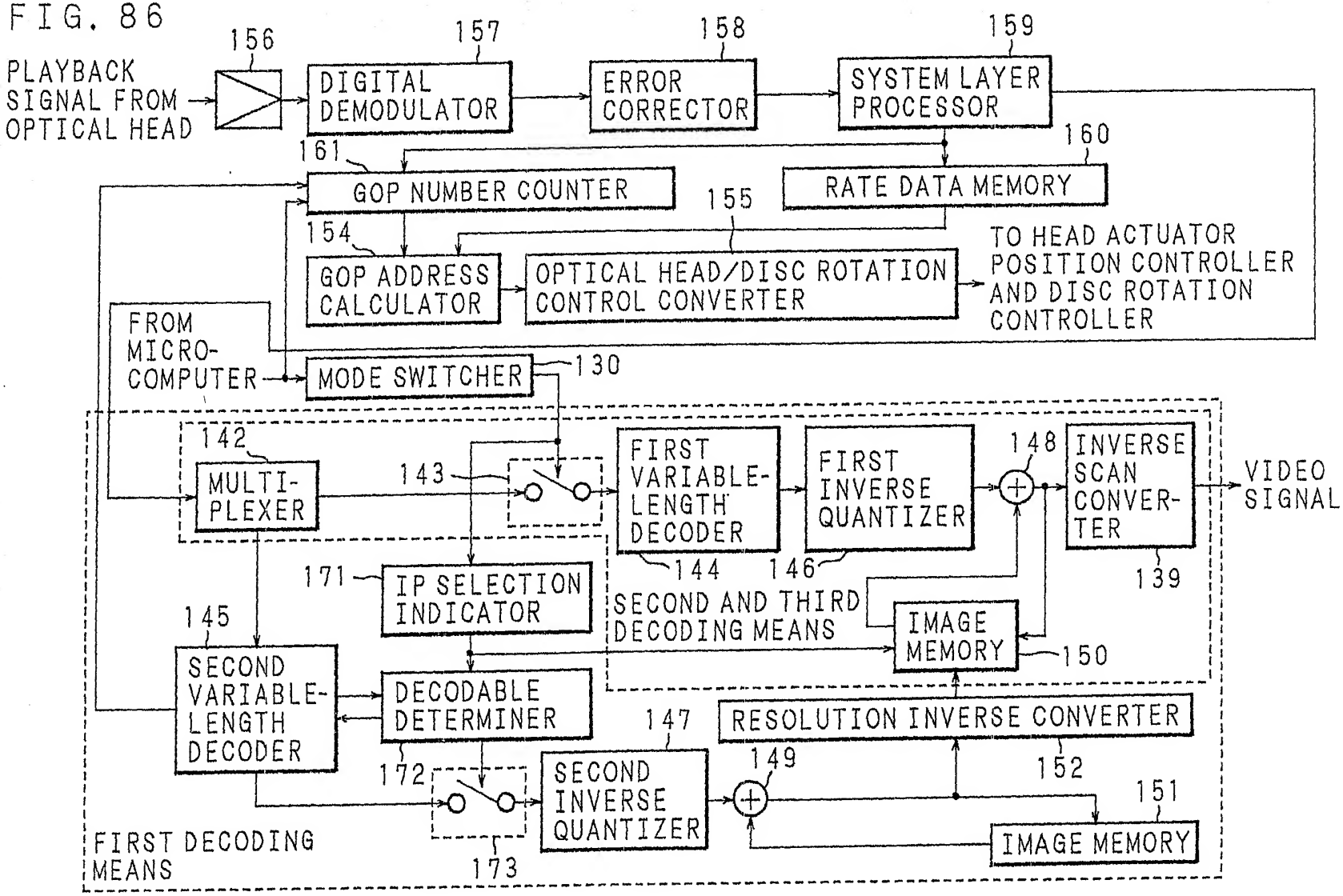
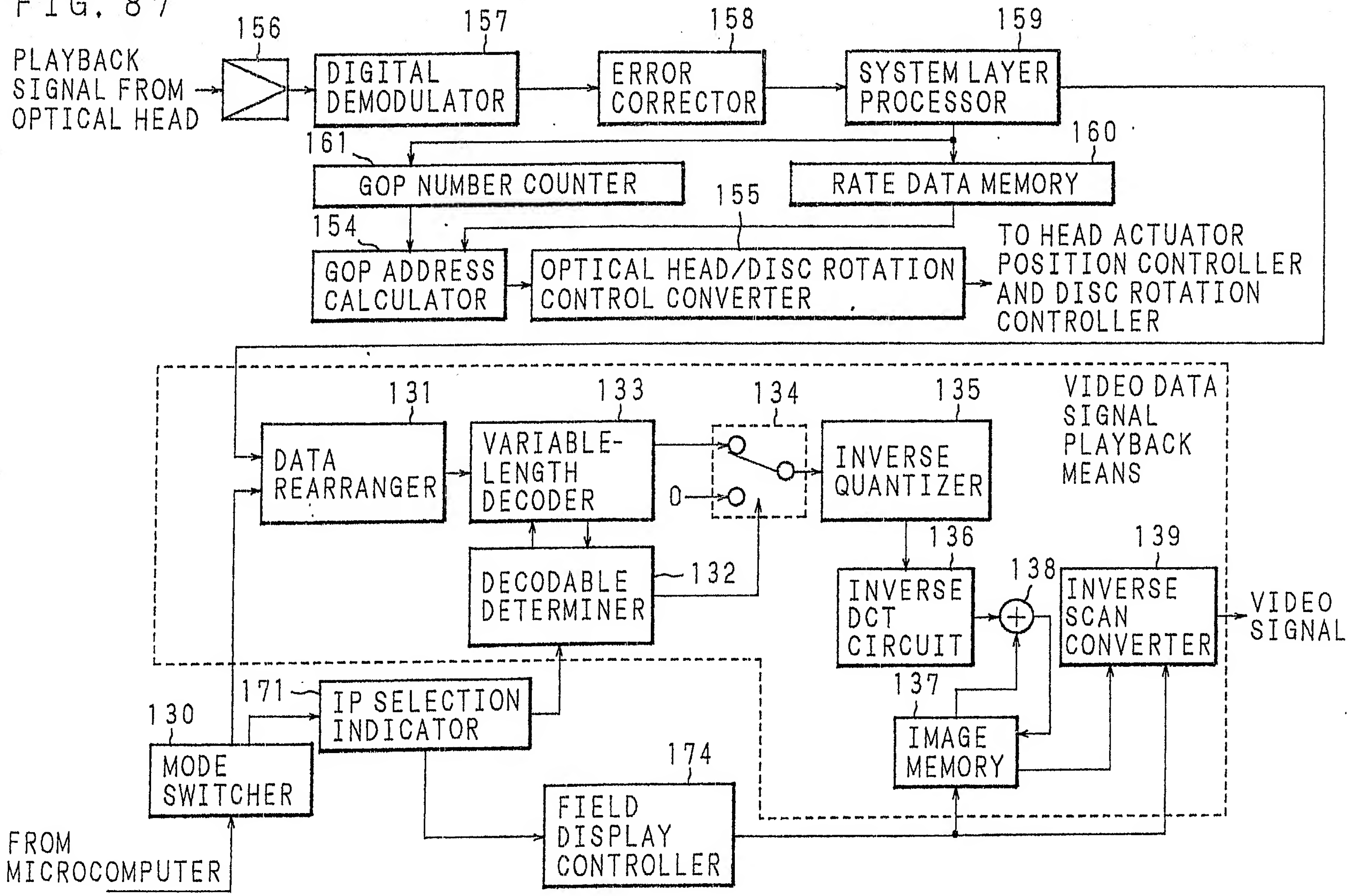

PLAYBACK SIGNAL FROM OPTICAL HEAD
156
DIGITAL DEMODULATOR
157
ERROR CORRECTOR
158
SYSTEM LAYER PROCESSOR
159
160
161
GOP NUMBER COUNTER
RATE DATA MEMORY
155
154
GOP ADDRESS CALCULATOR
OPTICAL HEAD/DISC ROTATION CONTROL CONVERTER
TO HEAD ACTUATOR POSITION CONTROLLER AND DISC ROTATION CONTROLLER
FROM MICRO-COMPUTER
MODE SWITCHER
130
142
MULTI-PLEXER
143
FIRST VARIABLE-LENGTH DECODER
FIRST INVERSE QUANTIZER
148
INVERSE SCAN CONVER-TER
VIDEO SIGNAL
144
146
139
171
IP SELECTION INDICATOR
SECOND AND THIRD DECODING MEANS
IMAGE MEMORY
150
145
SECOND VARIABLE-LENGTH DECODER
DECODABLE DETERMINER
147
RESOLUTION INVERSE CONVERTER
172
SECOND INVERSE QUANTIZER
149
152
151
IMAGE MEMORY
FIRST DECODING MEANS
173

FIG. 87



PLAYBACK SIGNAL FROM OPTICAL HEAD
156
157
DIGITAL DEMODULATOR
158
ERROR CORRECTOR
159
SYSTEM LAYER PROCESSOR
160
RATE DATA MEMORY
161
GOP NUMBER COUNTER
154
GOP ADDRESS CALCULATOR
155
OPTICAL HEAD/DISC ROTATION CONTROL CONVERTER
TO HEAD ACTUATOR POSITION CONTROLLER AND DISC ROTATION CONTROLLER
VIDEO DATA SIGNAL PLAYBACK MEANS
131
DATA REARRANGER
133
VARIABLE-LENGTH DECODER
134
0
135
INVERSE QUANTIZER
132
DECODABLE DETERMINER
136
INVERSE DCT CIRCUIT
138
139
INVERSE SCAN CONVERTER
VIDEO SIGNAL
137
IMAGE MEMORY
130
MODE SWITCHER
171
IP SELECTION INDICATOR
174
FIELD DISPLAY CONTROLLER
FROM MICROCOMPUTER

FIG. 88

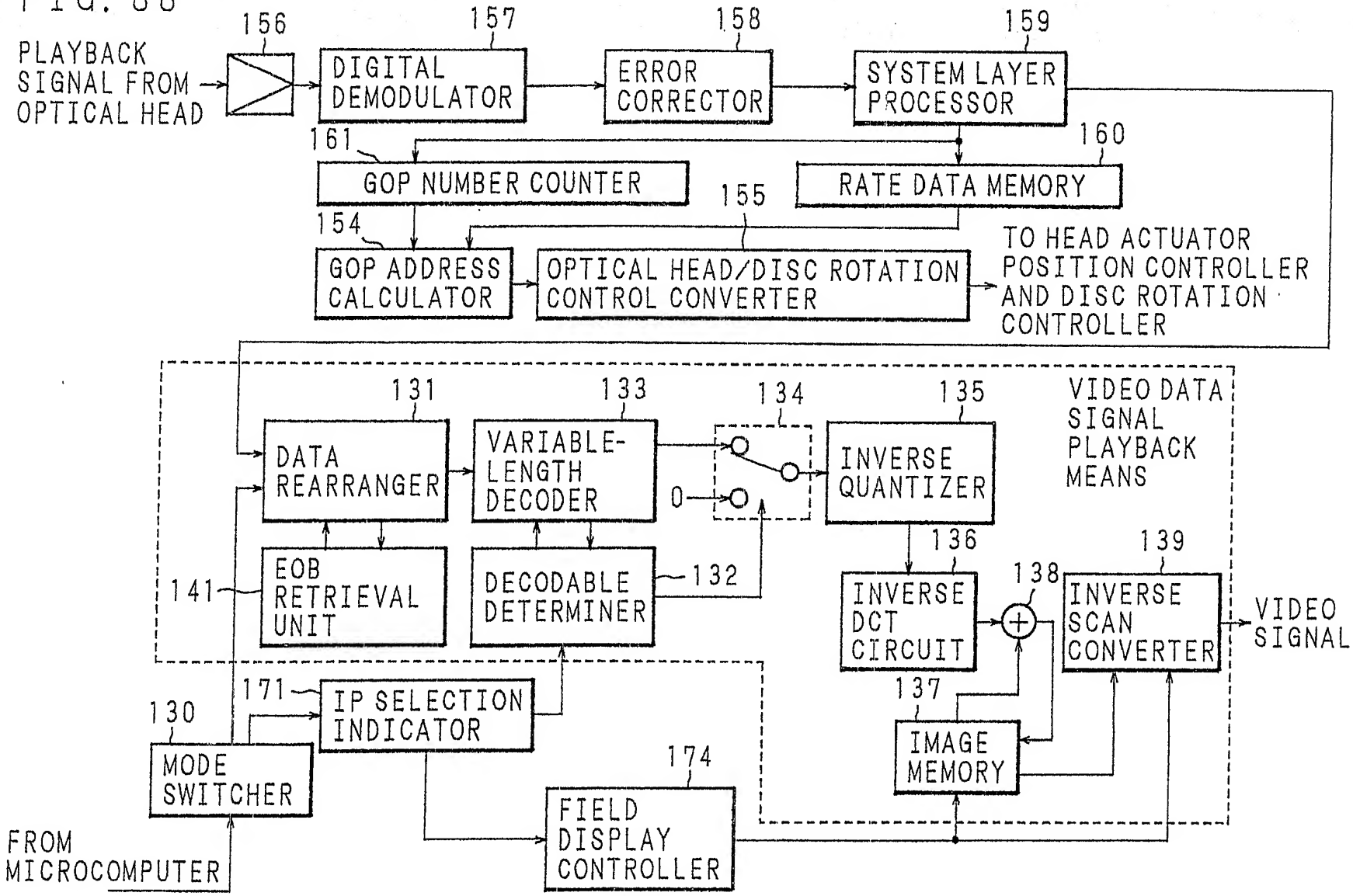

PLAYBACK SIGNAL FROM OPTICAL HEAD
156
157
DIGITAL DEMODULATOR
158
ERROR CORRECTOR
159
SYSTEM LAYER PROCESSOR
161
GOP NUMBER COUNTER
160
RATE DATA MEMORY
155
154
GOP ADDRESS CALCULATOR
OPTICAL HEAD/DISC ROTATION CONTROL CONVERTER
TO HEAD ACTUATOR POSITION CONTROLLER AND DISC ROTATION CONTROLLER
131
133
134
135
VIDEO DATA SIGNAL PLAYBACK MEANS
DATA REARRANGER
VARIABLE-LENGTH DECODER
0
INVERSE QUANTIZER
136
139
141
EOB RETRIEVAL UNIT
DECODABLE DETERMINER
132
138
INVERSE DCT CIRCUIT
INVERSE SCAN CONVERTER
VIDEO SIGNAL
171
IP SELECTION INDICATOR
137
130
MODE SWITCHER
IMAGE MEMORY
174
FIELD DISPLAY CONTROLLER
FROM MICROCOMPUTER

FIG. 89A

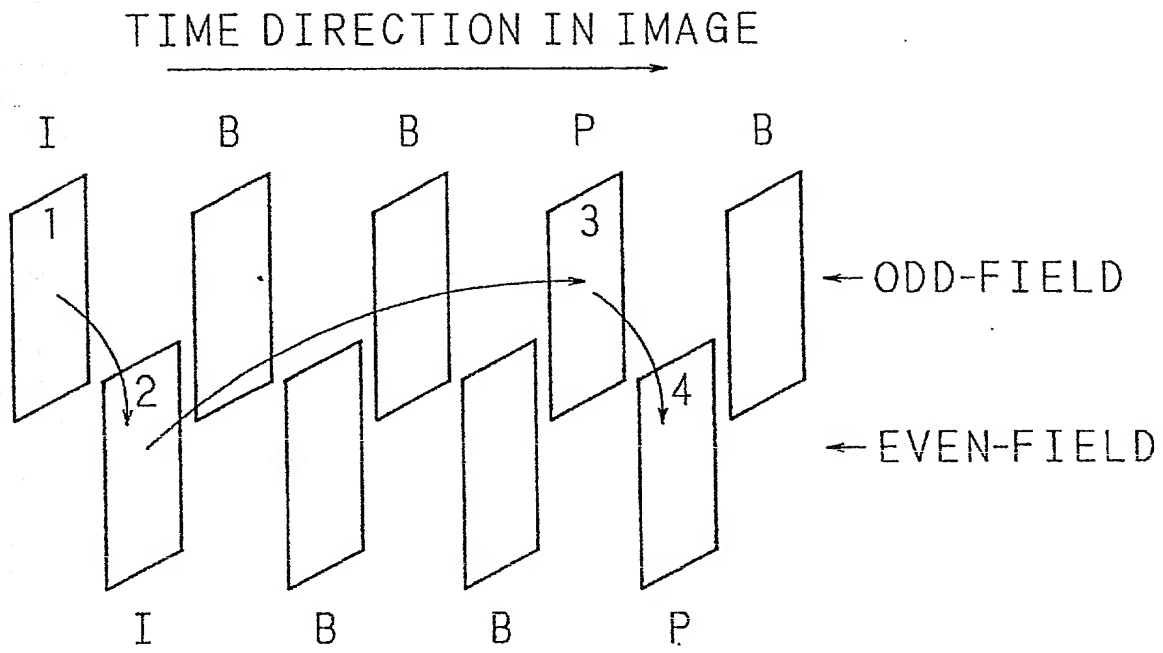


FIG. 89B

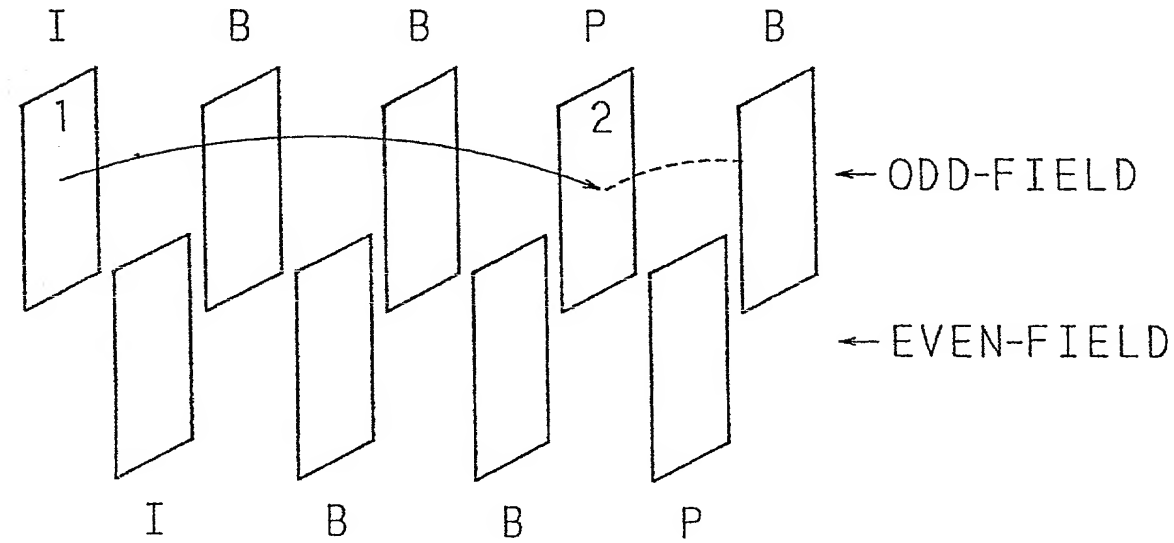


FIG. 90A

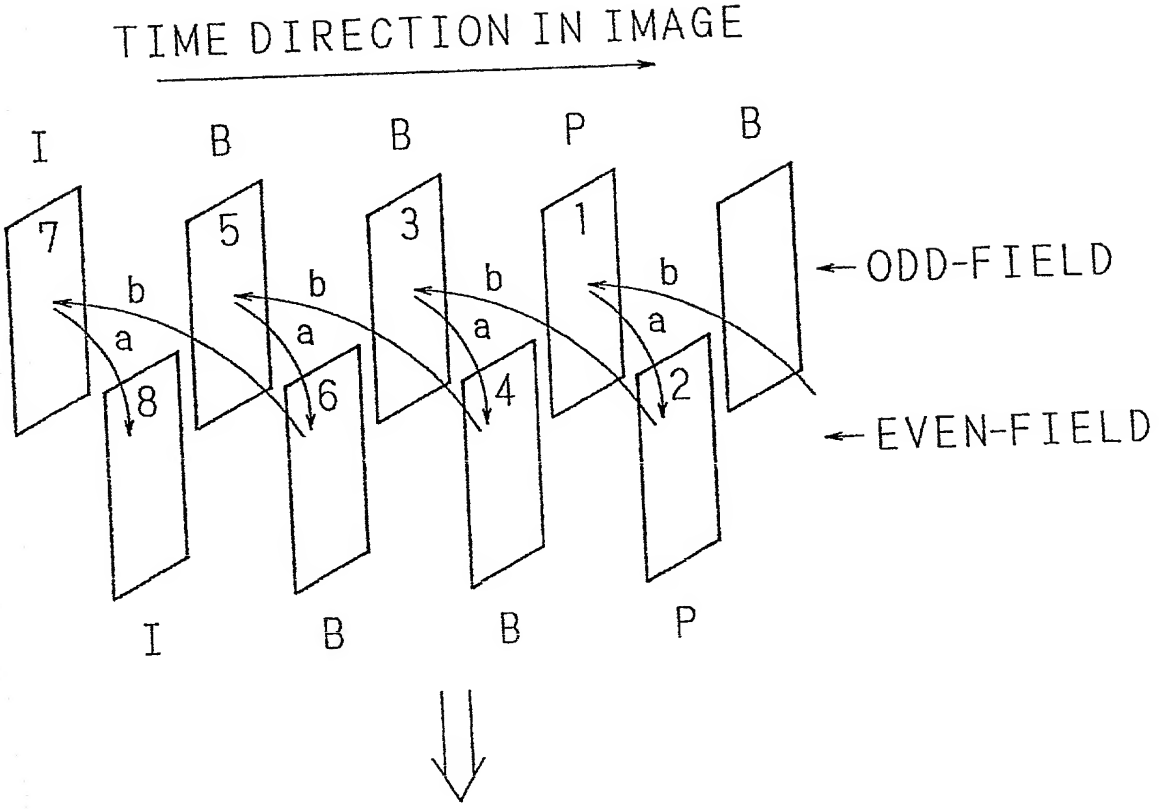


FIG. 90B